Memory FeRAM

1 M Bit (64 K × 16)

MB85R1002A

■ DESCRIPTIONS

The MB85R1002A is an FeRAM (Ferroelectric Random Access Memory) chip consisting of 65,536 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R1002A is able to retain data without using a back-up battery, as is needed for SRAM. The memory cells used in the MB85R1002A can be used for 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM. The MB85R1002A uses a pseudo-SRAM interface.

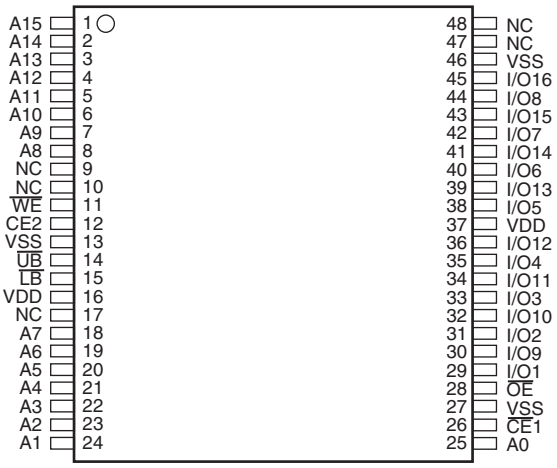
■ FEATURES

- Bit configuration : 65,536 words × 16 bits
- LB and UB data byte control
- Read/write endurance : 10^{10} times / byte
- Data retention : 10 years (+ 55 °C), 55 years (+ 35 °C)
- Operating power supply voltage : 3.0 V to 3.6 V
- Low power operation : Operating power supply current 10 mA (Typ)
  Standby current 10 μA (Typ)
- Operation ambient temperature range : − 40 °C to + 85 °C
- Package : 48-pin plastic TSOP
  RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

■ PIN ASSIGNMENTS

(TOP VIEW)

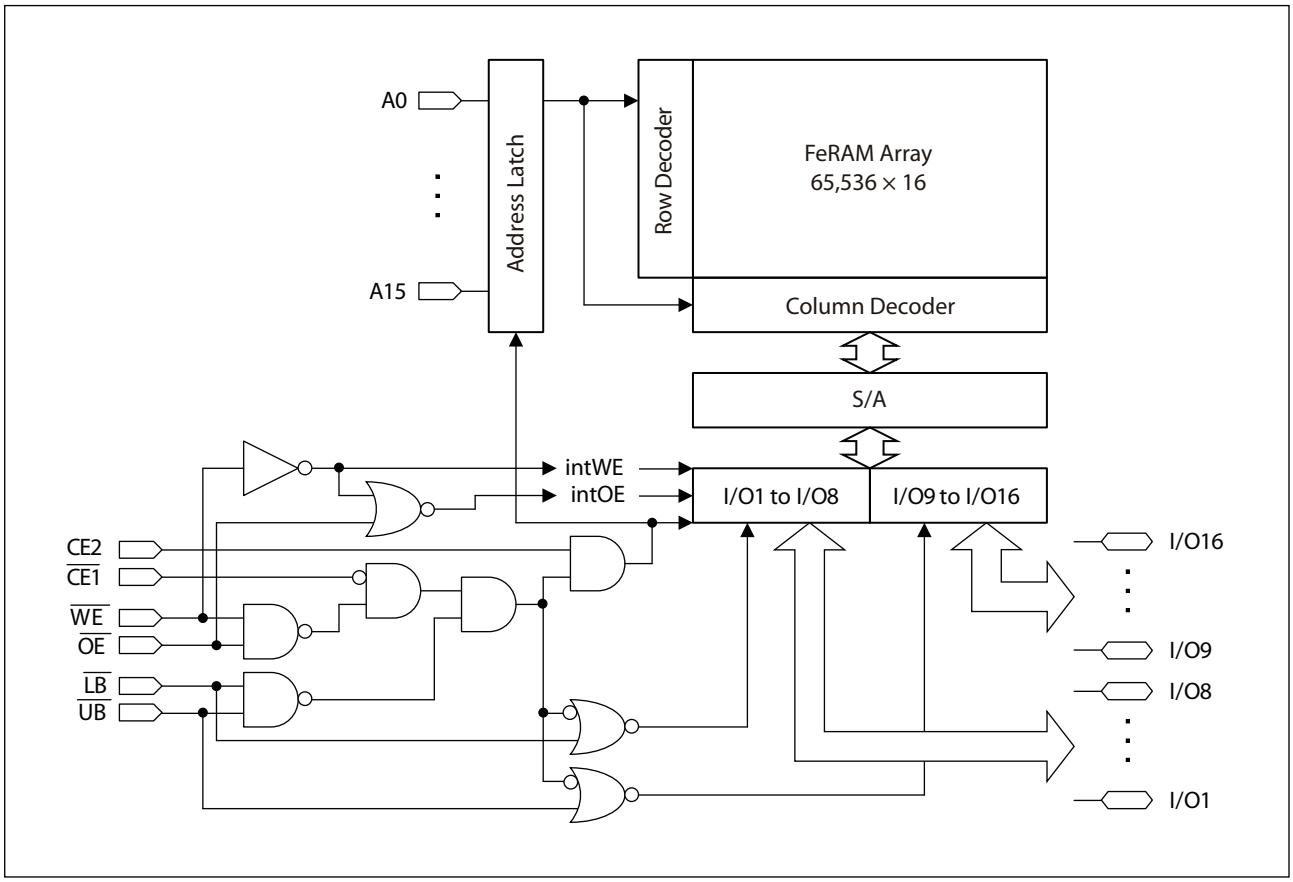


(TSOP 48)

■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 8, 18 to 25	A0 to A15	Address Input pins
29 to 36, 38 to 45	I/O1 to I/O16	Data Input/Output pins
26	$\overline{CE1}$	Chip Enable 1 Input pin
12	CE2	Chip Enable 2 Input pin
11	$\overline{WE}$	Write Enable Input pin
28	$\overline{OE}$	Output Enable Input pin
14, 15	$\overline{LB}$, $\overline{UB}$	Data Byte Control Input pins
16, 37	VDD	Supply Voltage pins Connect all two pins to the power supply.
13, 27, 46	VSS	Ground pins Connect all three pins to ground.
9, 10, 17, 47, 48	NC	No Connect pins Leave these pins open, or connect to VDD or VSS.

■ BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	Supply Current
Standby Precharge	H	X	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
	X	L	X	X	X	X			
	X	X	H	H	X	X			
	X	X	X	X	H	H			
Read	↓	H	H	L	L	L	Data Output	Data Output	Operation (I_{DD})
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
	L	↑	H	L	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Read (Pseudo-SRAM, $\overline{OE}$ control*1)	L	H	H	↓	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Write	↓	H	L	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	
	L	↑	L	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	
Write (Pseudo-SRAM, $\overline{WE}$ control*2)	L	H	↓	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	

Note: L = V_{IL}, H = V_{IH}, X can be either H, L, ↓ or ↑, Hi-Z = High Impedance

↓ : Latch address and latch data at falling edge, ↑ : Latch address and latch data at rising edge

*1 : $\overline{OE}$ control of the Pseudo-SRAM means the valid address at the falling edge of $\overline{OE}$ to read.

*2 : $\overline{WE}$ control of the Pseudo-SRAM means the valid address and data at the falling edge of $\overline{WE}$ to write.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V_{DD}	–0.5	+4.0	V
Input Pin Voltage*	V_{IN}	–0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V_{OUT}	–0.5	V_{DD} + 0.5 (≤ 4.0)	V
Operation ambient temperature	T_A	–40	+85	°C
Storage Temperature	T_{STG}	–55	+125	°C

* : All voltages are referenced to VSS = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*1	V_{DD}	3.0	3.3	3.6	V
Operation ambient temperature*2	T_A	– 40	—	+85	°C

*1 : All voltages are referenced to VSS = 0 V.

*2 : Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{DD}	—	—	10	μA
Output Leakage Current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{DD}, $\overline{CE}1$ = V_{IH} or $\overline{OE}$ = V_{IH}	—	—	10	μA
Operating Power Supply Current*1	I_{DD}	$\overline{CE}1$ = 0.2 V, CE2 = V_{DD} – 0.2 V, I_{out} = 0 mA	—	10	15	mA
Standby Current*2	I_{SB}	$\overline{CE}1 \geq V_{DD} - 0.2$ V CE2 ≤ 0.2 V $\overline{OE} \geq V_{DD} - 0.2$ V, $\overline{WE} \geq V_{DD} - 0.2$ V $\overline{LB} \geq V_{DD} - 0.2$ V, $\overline{UB} \geq V_{DD} - 0.2$ V	—	10	50	μA
High Level Input Voltage	V_{IH}	V_{DD} = 3.0 V to 3.6 V	$V_{DD} \times 0.8$	—	V_{DD} + 0.5 (≤ 4.0)	V
Low Level Input Voltage	V_{IL}	V_{DD} = 3.0 V to 3.6 V	–0.5	—	+0.6	V
High Level Output Voltage	V_{OH}	I_{OH} = – 1.0 mA	$V_{DD} \times 0.8$	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.0 mA	—	—	0.4	V

*1 : During the measurement of I_{DD}, the Address, Data In were taken to only change once per active cycle.
Iout : output current

*2 : All pins other than setting pins should be input at the CMOS level voltages such as H ≥ V_{DD} – 0.2 V, L ≤ 0.2 V.

2. AC Characteristics

• AC Test Conditions

Supply Voltage	: 3.0 V to 3.6 V
Operation Ambient Temperature	: –40 °C to +85 °C
Input Voltage Amplitude	: 0.3 V to 2.7 V
Input Rising Time	: 5 ns
Input Falling Time	: 5 ns
Input Evaluation Level	: 2.0 V / 0.8 V
Output Evaluation Level	: 2.0 V / 0.8 V
Output Load Capacitance	: 50 pF

(1) Read Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle time	t_{RC}	150	—	ns
$\overline{CE1}$ Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
$\overline{OE}$ Active Time	t_{RP}	120	—	ns
$\overline{LB}$, $\overline{UB}$ Active Time	t_{BP}	120	—	ns
Precharge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
$\overline{OE}$ Setup Time	t_{ES}	0	—	ns
$\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	5	—	ns
Output Data Hold time	t_{OH}	0	—	ns
Output Set Time	t_{LZ}	30	—	ns
$\overline{CE1}$ Access Time	t_{CE1}	—	100	ns
CE2 Access Time	t_{CE2}	—	100	ns
$\overline{OE}$ Access Time	t_{OE}	—	100	ns
Output Floating Time	t_{OHZ}	—	20	ns

(2) Write Cycle

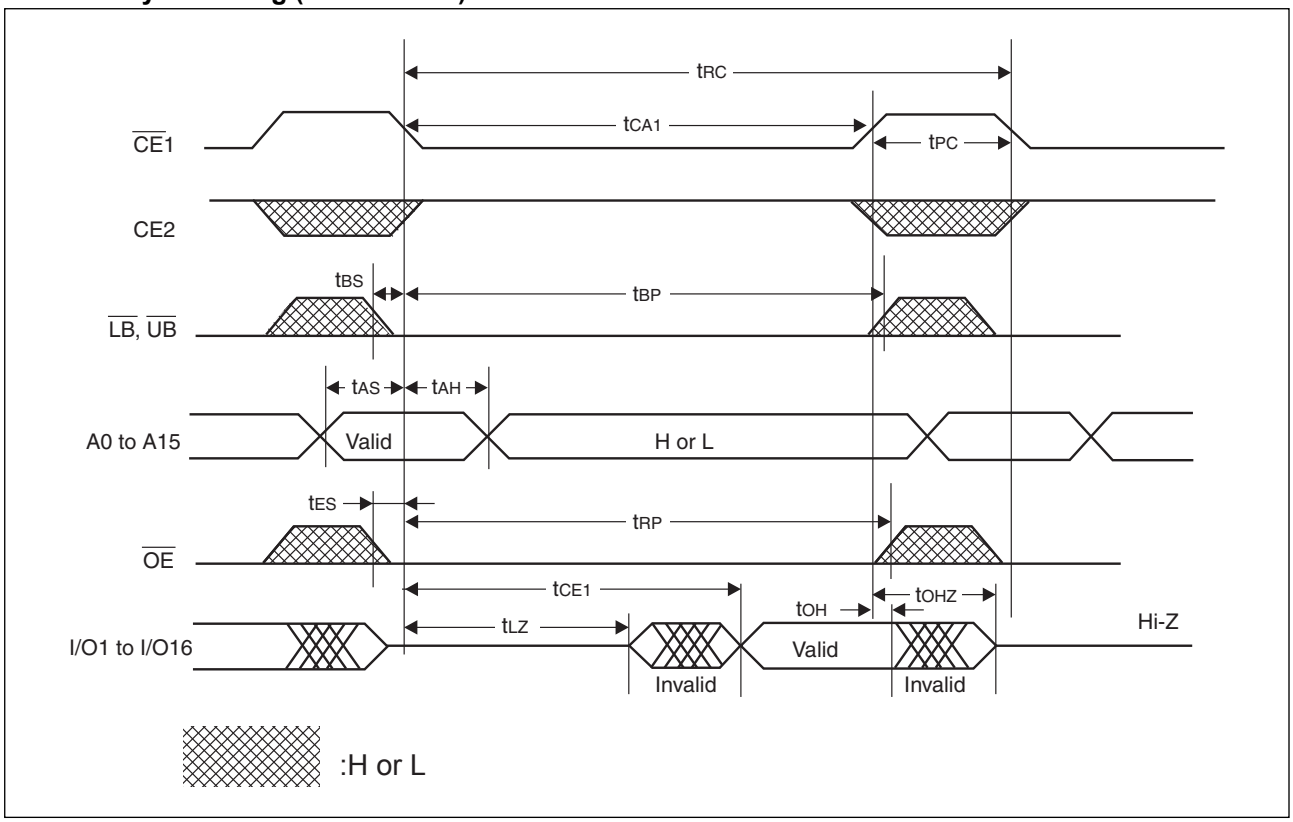
Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	150	—	ns
$\overline{CE}$1 Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
$\overline{LB}$, $\overline{UB}$ Active Time	t_{BP}	120	—	ns
Precharge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
$\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	5	—	ns
Write Pulse Width	t_{WP}	120	—	ns
Data Setup Time	t_{DS}	0	—	ns
Data Hold Time	t_{DH}	50	—	ns
Write Setup Time	t_{WS}	0	—	ns

3. Pin Capacitance

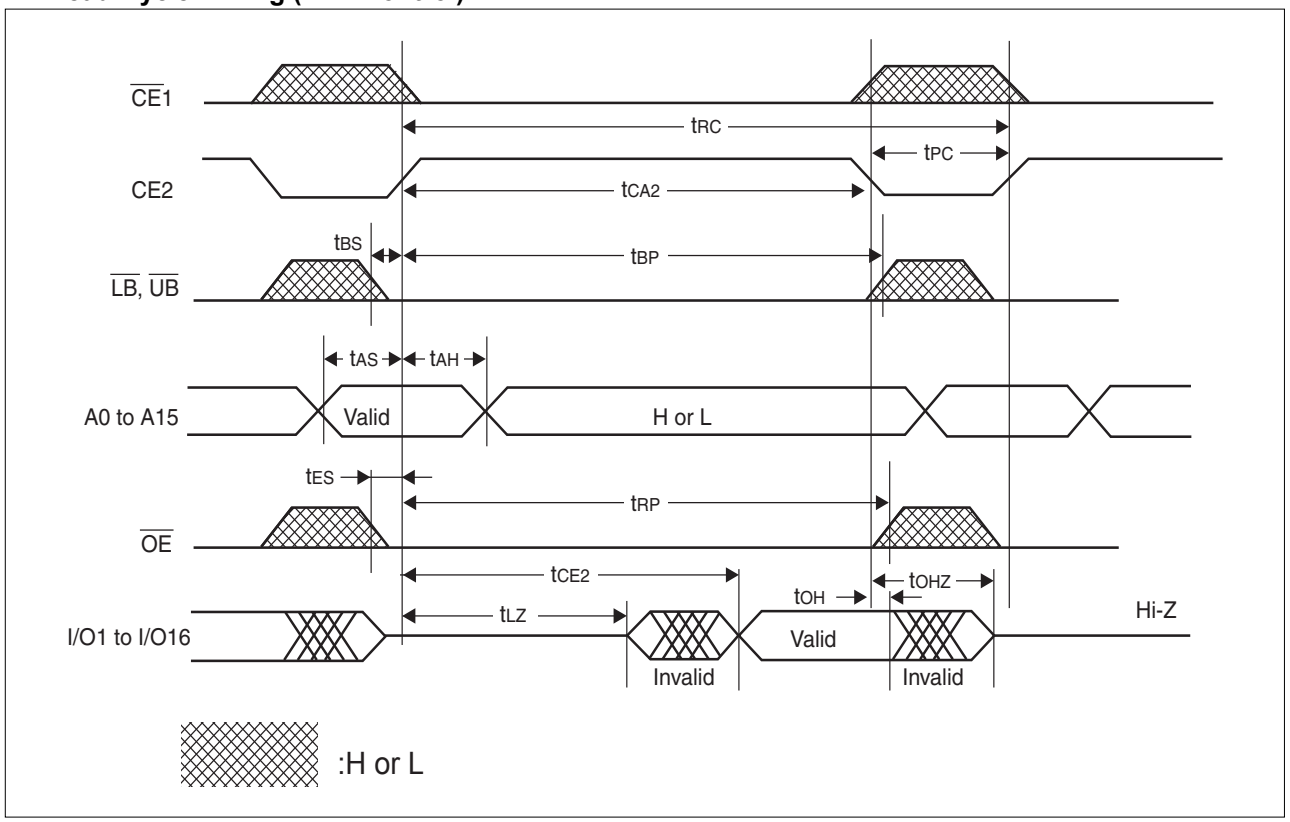
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{DD} = V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A = +25$ °C	—	—	10	pF
Output Capacitance	C_{OUT}		—	—	10	pF

■ TIMING DIAGRAMS

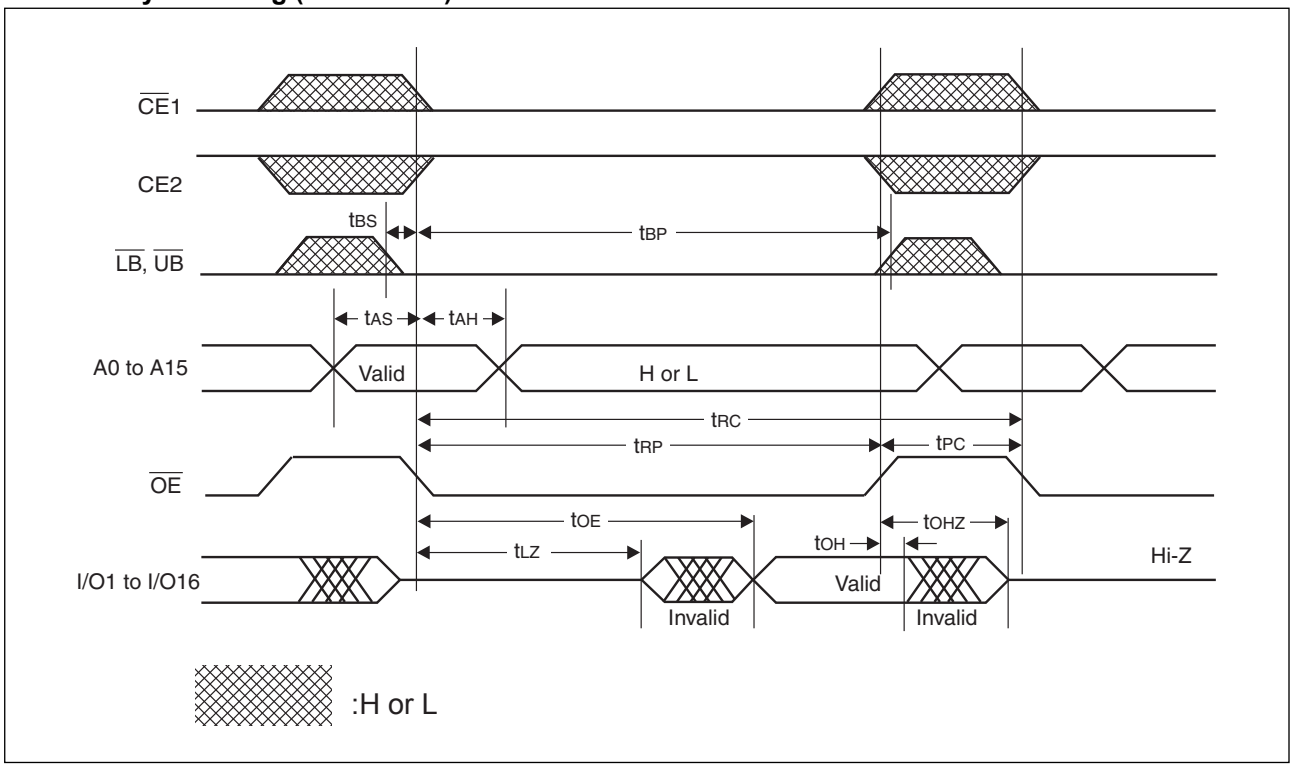
1. Read Cycle Timing ($\overline{CE1}$ Control)



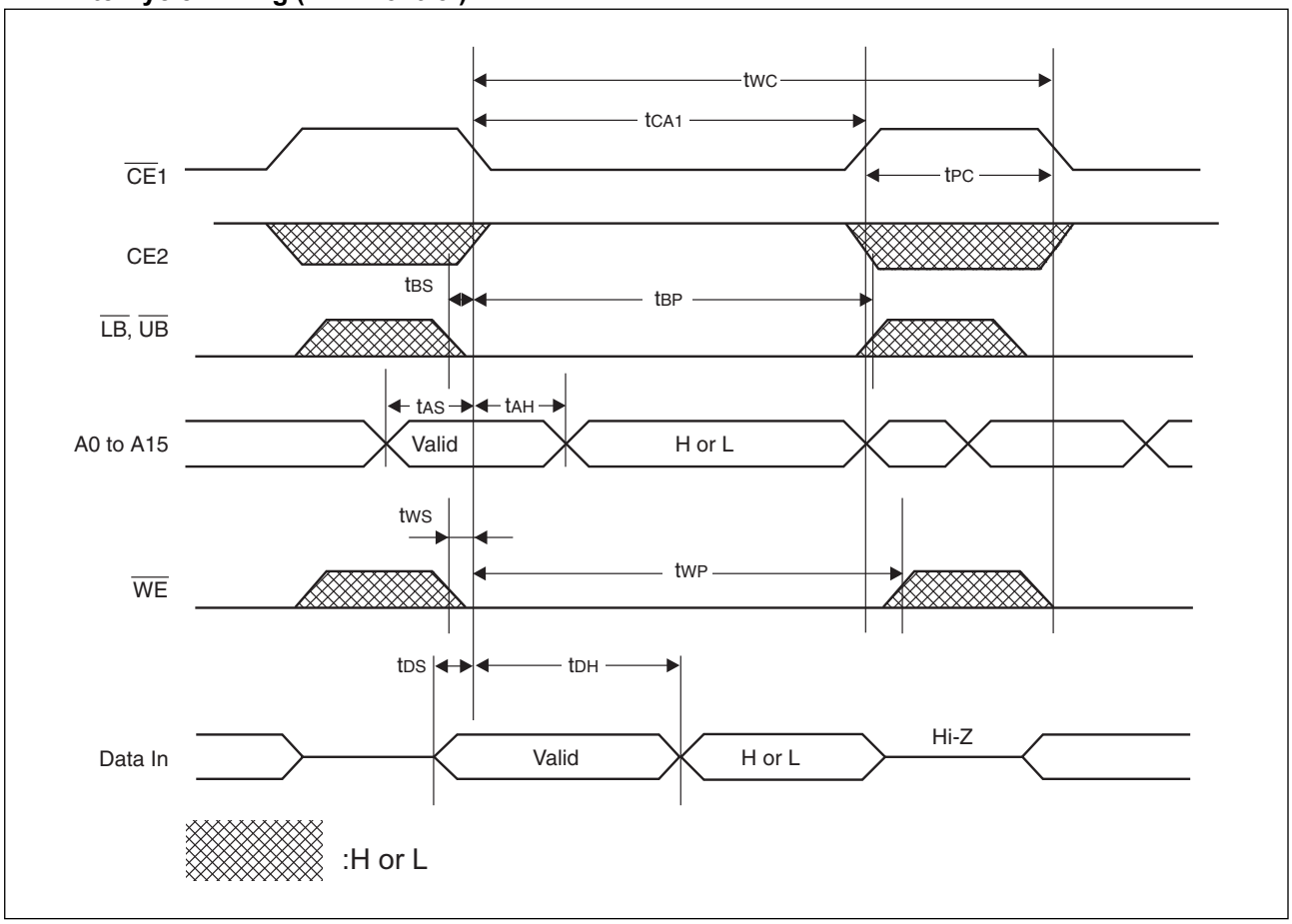
2. Read Cycle Timing (CE2 Control)



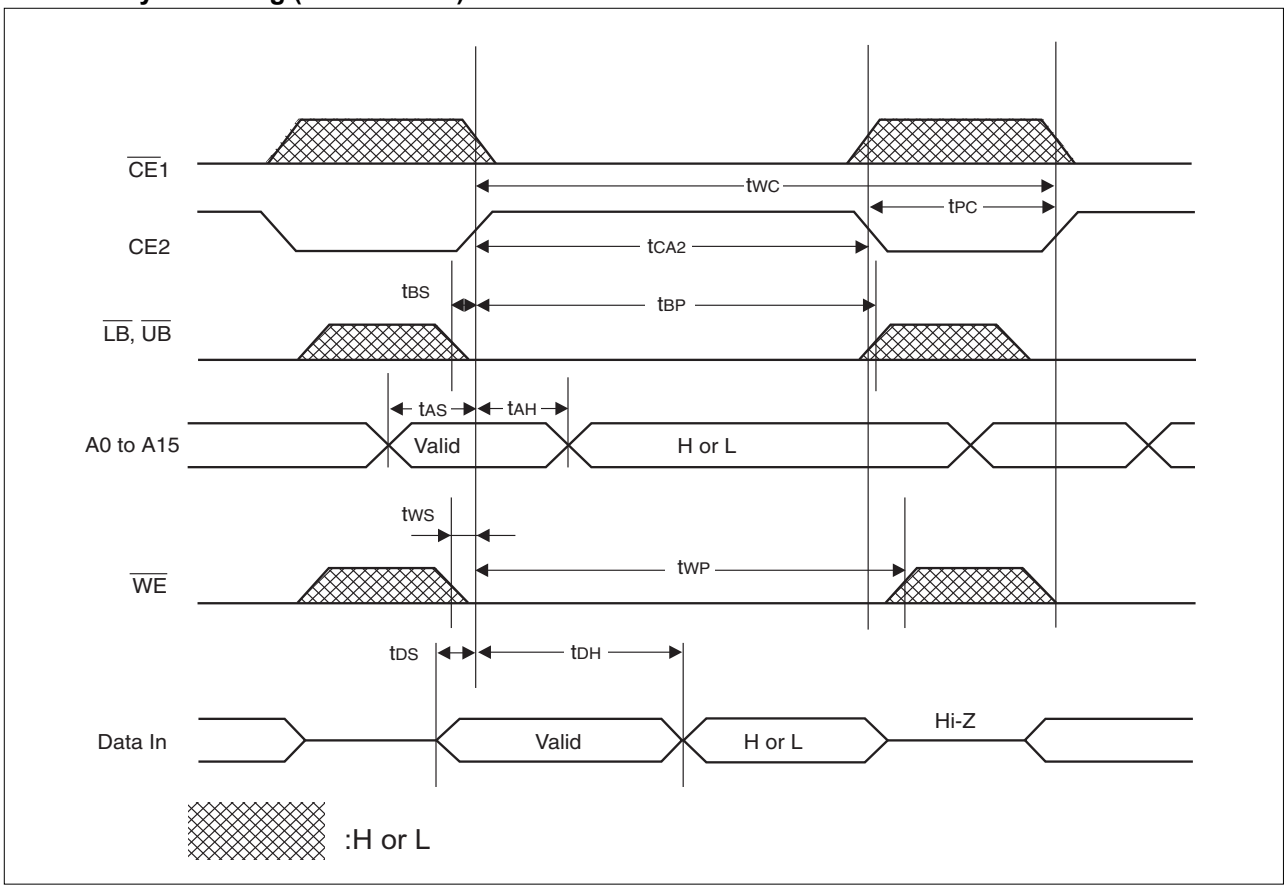
3. Read Cycle Timing ($\overline{OE}$ Control)



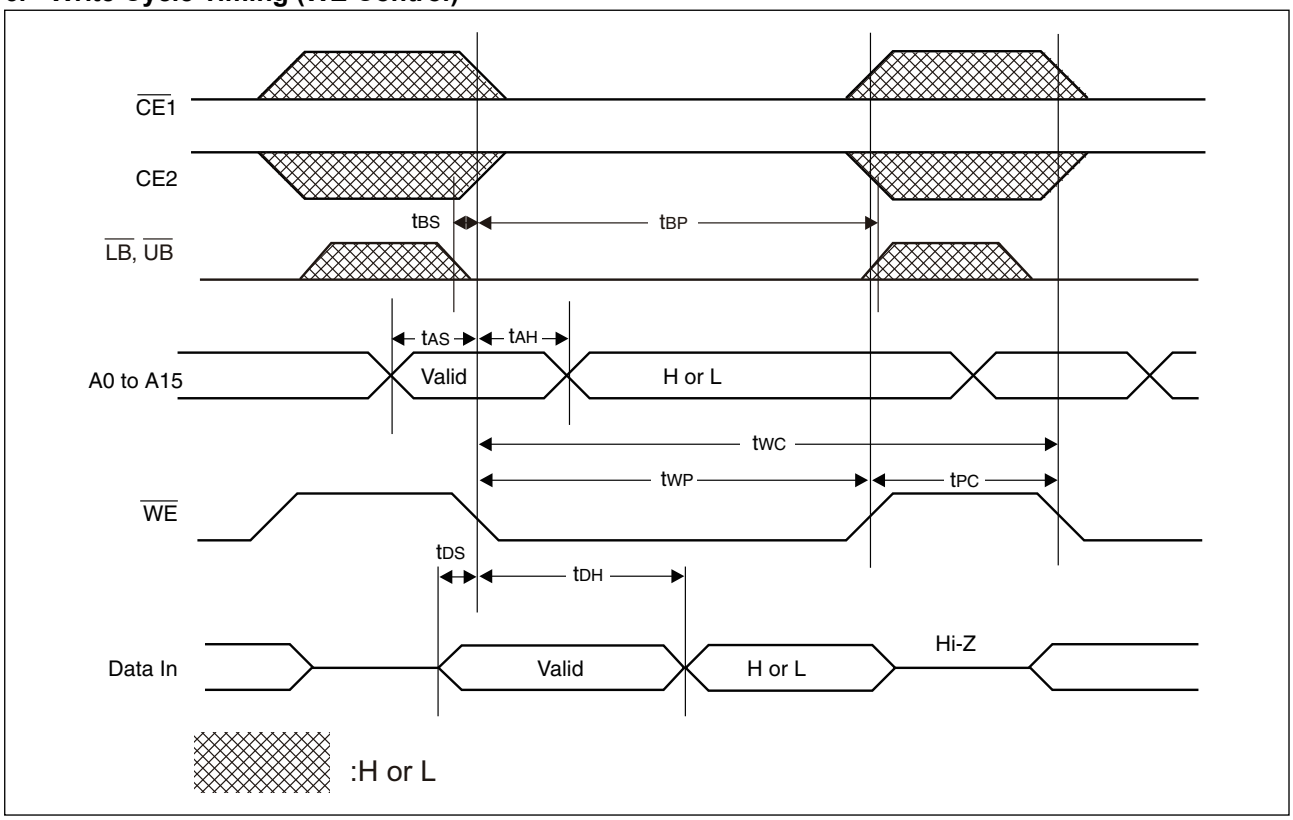
4. Write Cycle Timing ($\overline{CE1}$ Control)



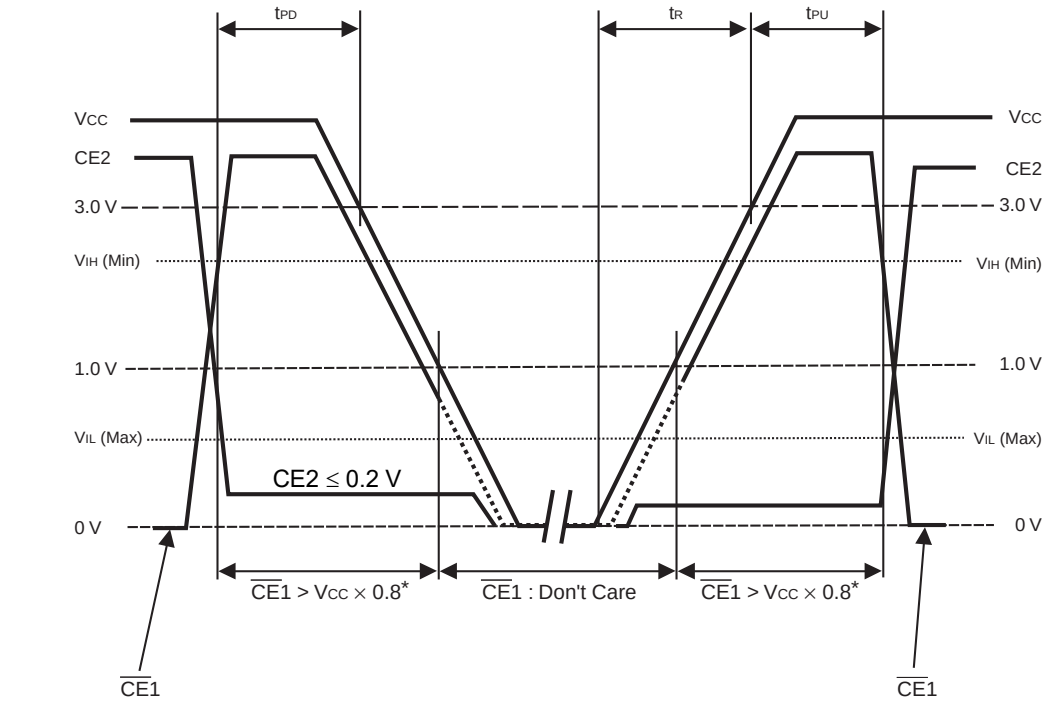
5. Write Cycle Timing (CE2 Control)



6. Write Cycle Timing ($\overline{WE}$ Control)



■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE}1$ level hold time for Power OFF	t_{PD}	85	—	—	ns
$\overline{CE}1$ level hold time for Power ON	t_{PU}	85	—	—	ns
Power supply rising time	t_R	0.05	—	200	ms

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.
In case the power is turned on or off, use the power supply reset IC and fix the CE2 to low level, to prevent unexpected writing. Use either of $\overline{CE}1$ or CE2, or both to disable control of the device.

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{10}	—	Times/byte	Operation Ambient Temperature T_A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 55 °C
	55	—		Operation Ambient Temperature T_A = + 35 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

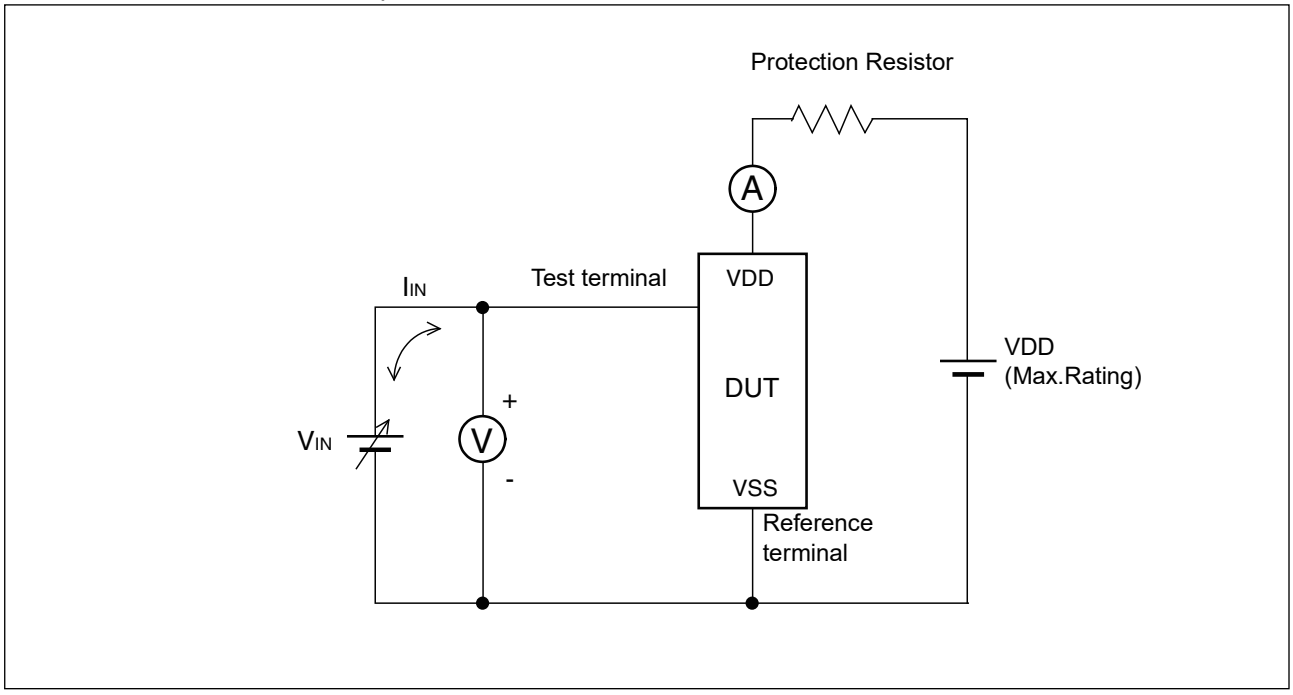
■ NOTES ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

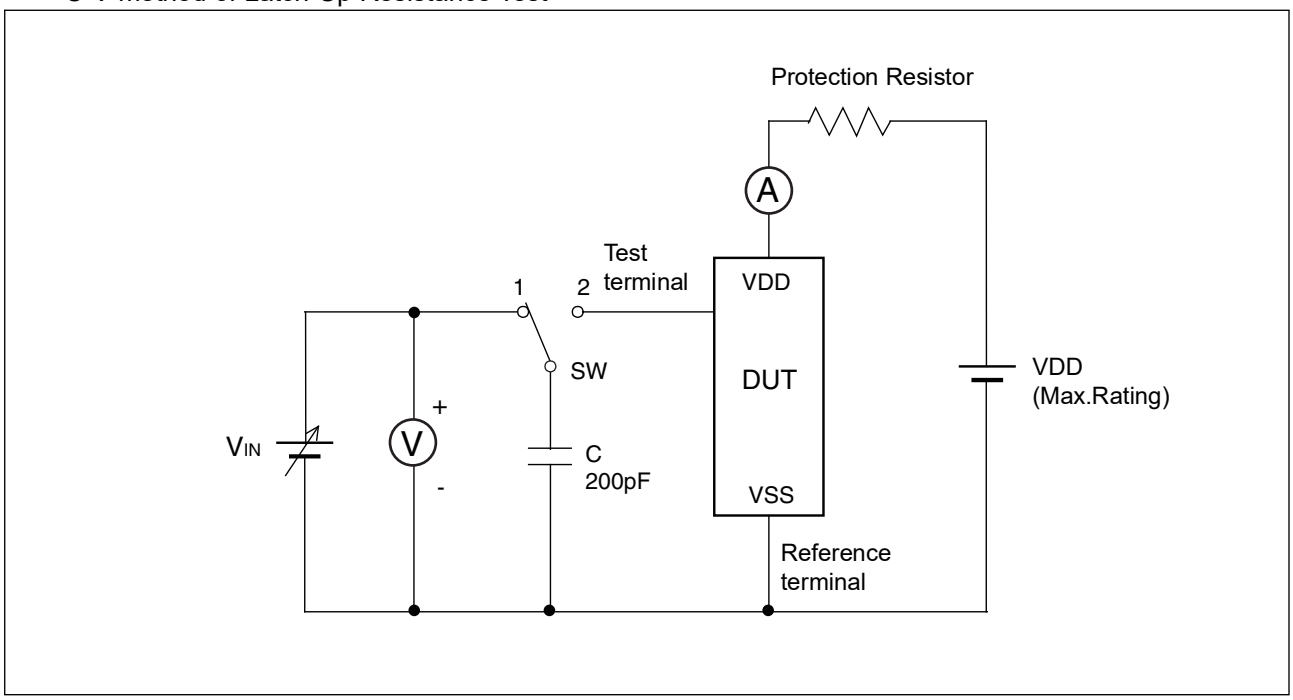
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85R1002ANC-GE1	≥ |2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥ |200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |1000 V|
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		≥ |300 mA|
Latch-Up (C-V Method) Proprietary method		—

- Current method of Latch-Up Resistance Test



Note : The voltage V_{IN} is increased gradually and the current I_{IN} of 300 mA at maximum shall flow.
Confirm the latch up does not occur under I_{IN} = ± 300 mA.
In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

• C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

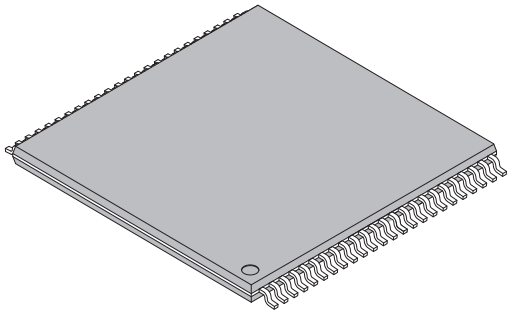
This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

■ ORDERING INFORMATION

Part Number	Package	Shipping form	Minimum shipping quantity
MB85R1002ANC-GE1	48-pin plastic TSOP	Tray	—*

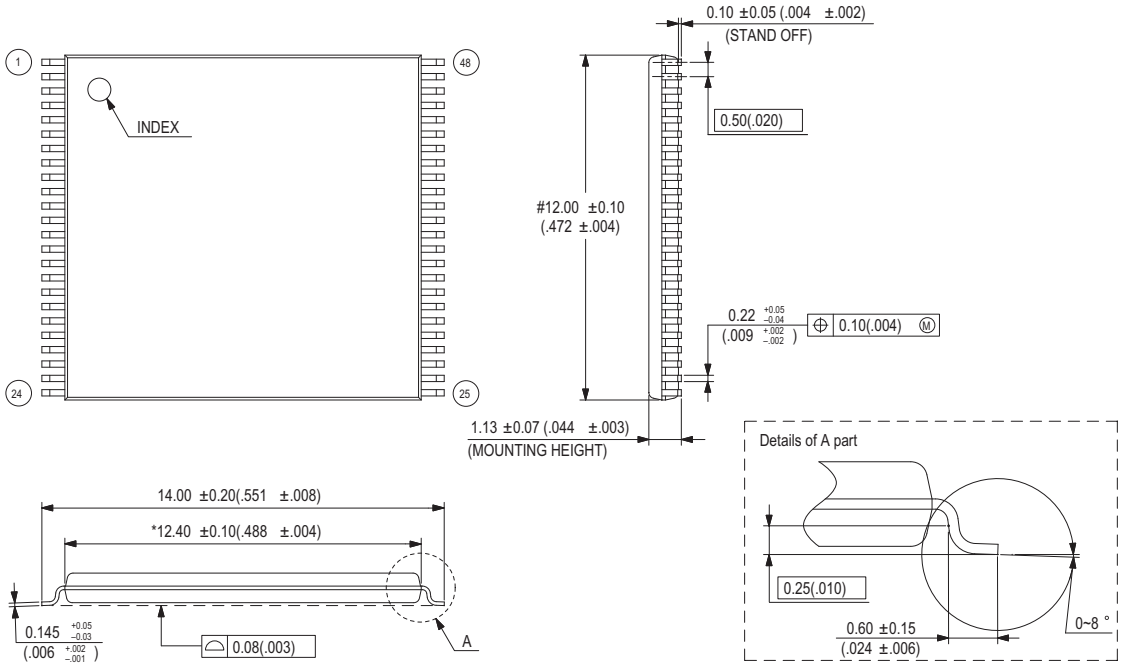
*: Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSIONS

48-pin plastic TSOP		
	Lead pitch	0.50 mm
	Pa ck age width × pa ck age length	12.00 mm × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
MB85R1002ANC-GE1		

48-pin plastic TSOP

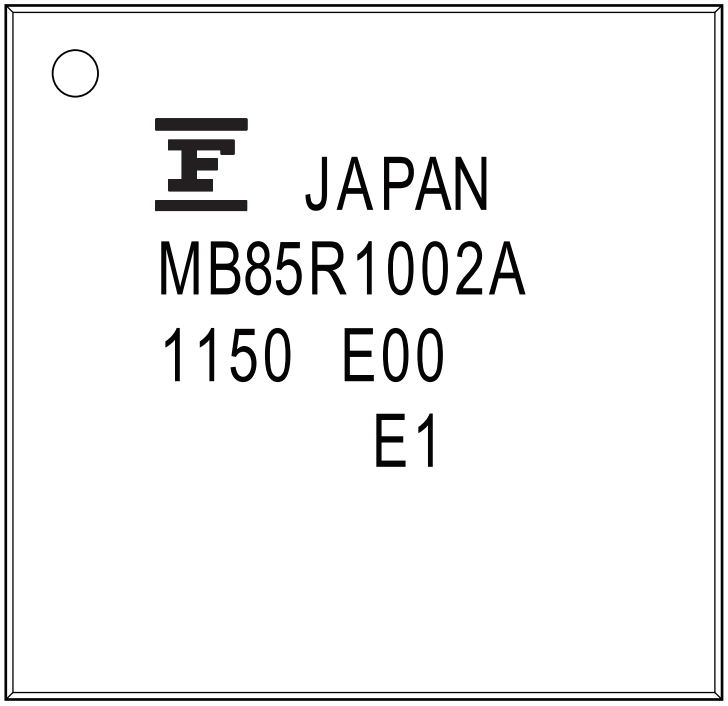
Note 1) # : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) * : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.

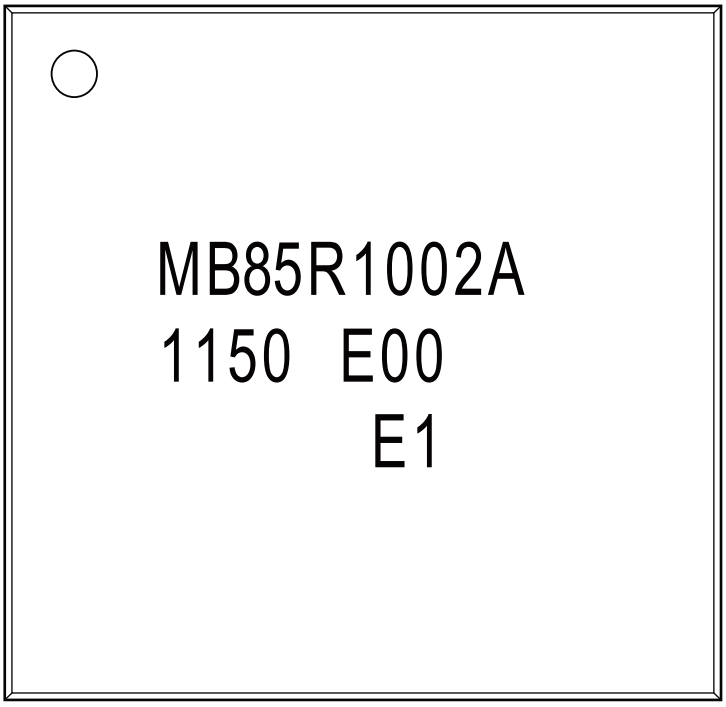


Di mensions in mm (inches).
No te: The values in parentheses are reference values.

■ **MARKING**(example)

[MB85R1002ANC-GE1]





[TSOP 48]

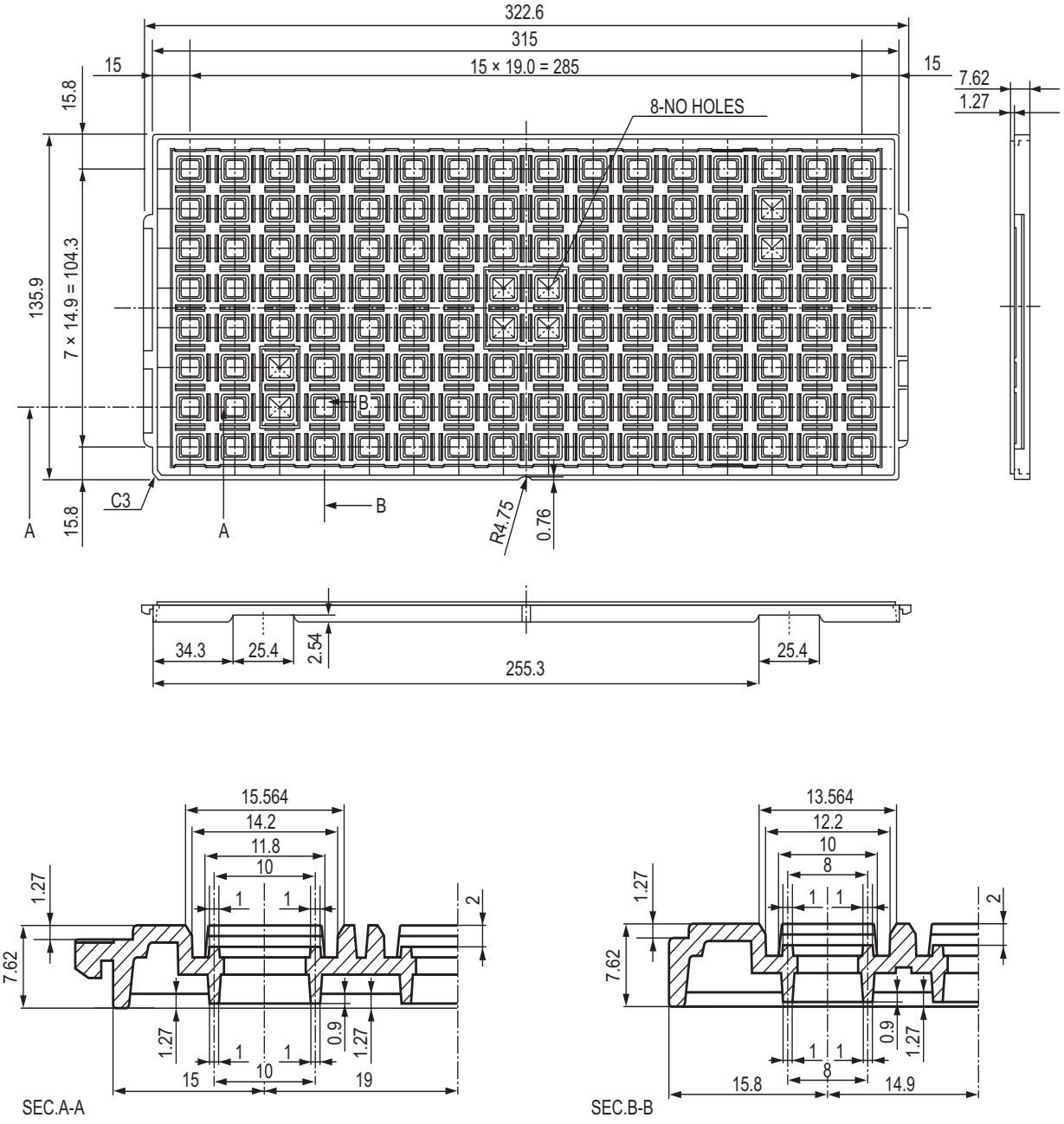
■ SHIPPING FORM

1. Tray

1.1 Tray Dimensions

TSOP48

Maximum storage capacity		
pcs/tray	pcs/inner box	pcs/outer box
128	1280	5120

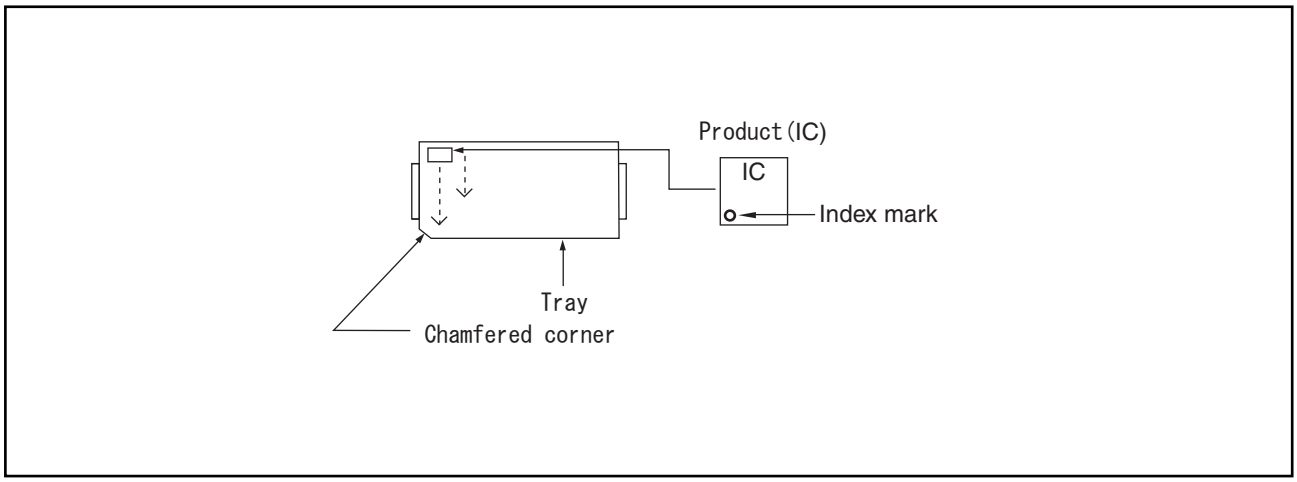


(Dimensions in mm)

Material : Conductive polyphenyleneether

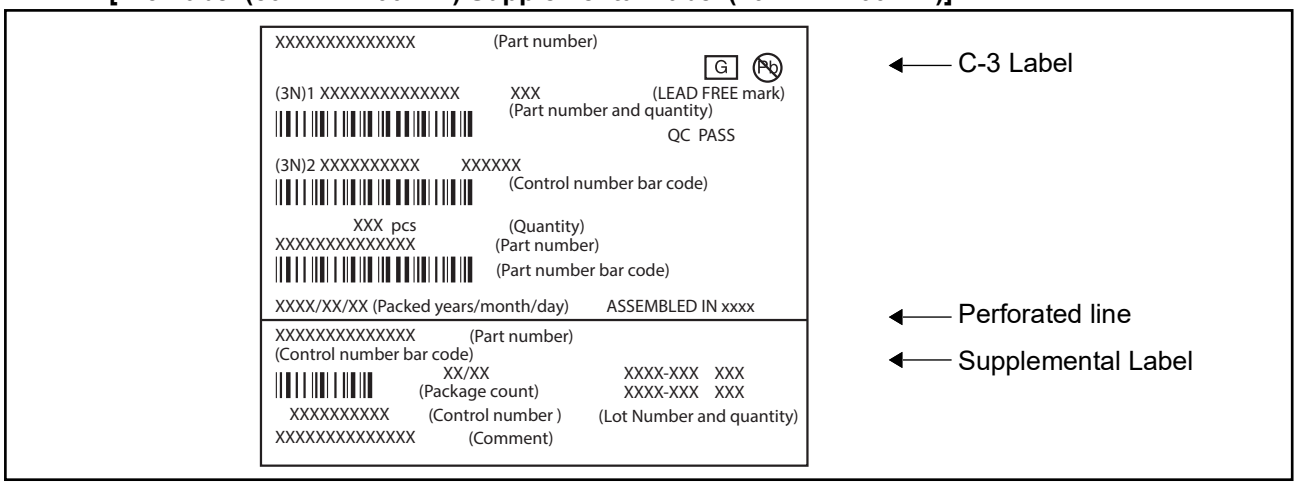
Heat proof temperature : 125 °C MAX

1.2 IC orientation



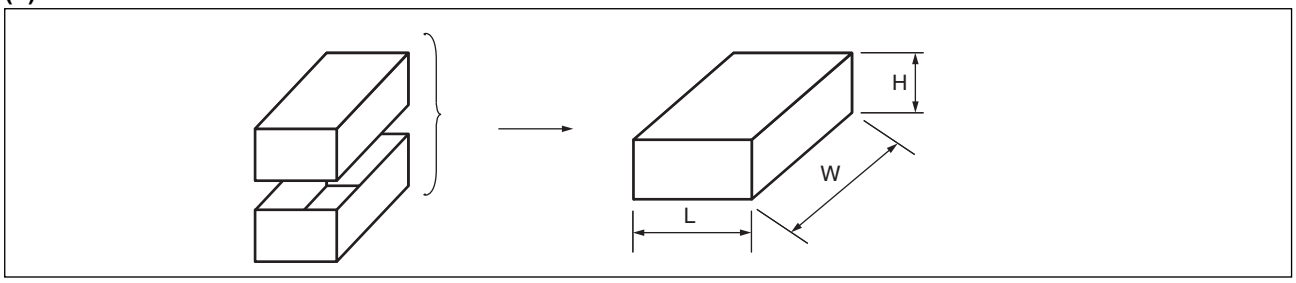
1.3 Product label indicators

Label l: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping) [C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



1.4 Dimensions for Containers

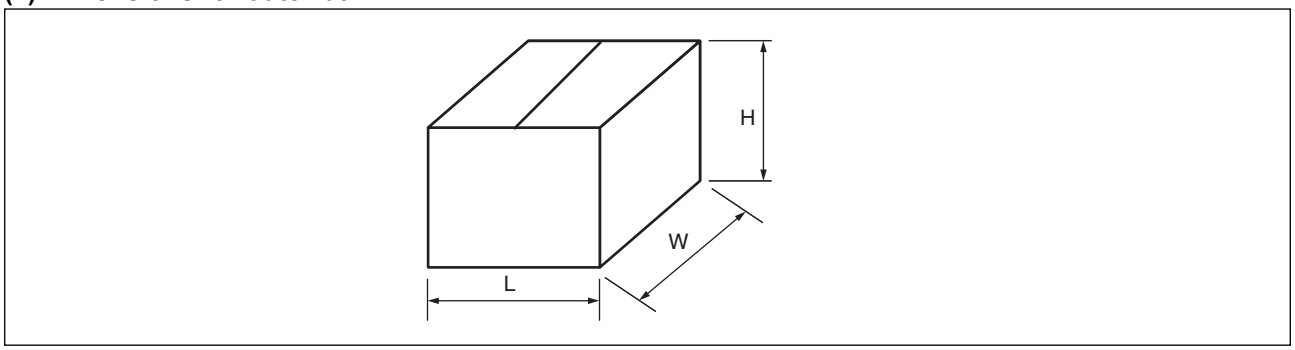
(1) Dimensions for inner box



L	W	H
165	360	75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
355	385	195

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
17	MARKING	New marking format is added.

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https://ramxeed.com/