

## Memory FeRAM

# 4 M (256 K × 16) Bit

## MS85R4M2TA

#### **■ DESCRIPTIONS**

The MS85R4M2TA is an FeRAM (Ferroelectric Random Access Memory) chip consisting of 262,144 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MS85R4M2TA is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MS85R4M2TA can be used for 10<sup>14</sup> read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MS85R4M2TA uses a pseudo-SRAM interface.

#### **■ FEATURES**

• Bit configuration :  $262,144 \text{ words} \times 16 \text{ bits}$ 

• LB and UB data byte control : Available Configuration of 524,288 words × 8 bits

• Read/write endurance :  $10^{14}$  times / 64 bits( + 85 °C),  $10^{13}$  times / 64 bits( + 105 °C),

• Data retention : 10 years ( + 105 °C), 40 years ( + 85 °C), over 200 years ( + 35 °C)

• Operating power supply voltage : 1.8 V to 3.6 V

• Low power operation : Operating power supply current 16 mA (Max)

Standby current 150 μA (Max) Sleep current 12 μA (Max)

• Operation ambient temperature range : -40 °C to +105 °C

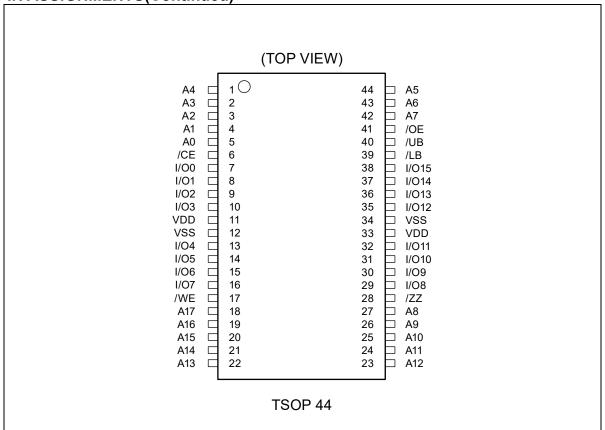
• Package : 44-pin plastic TSOP

RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

### **■ PIN ASSIGNMENTS**

**PIN ASSIGNMENTS(Continued)** 

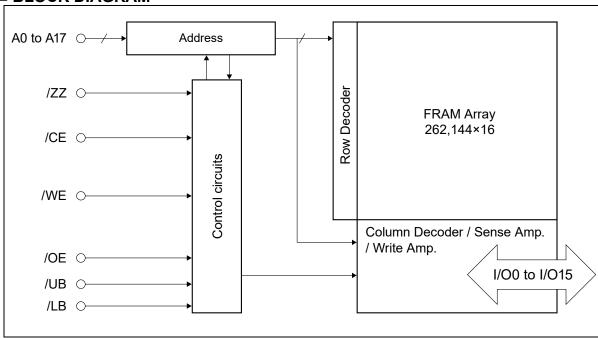


## ■ PIN DESCRIPTIONS

Pin Number(TSOP)	Pin Name	Functional Description
5 to 1, 44 to 42,	A0 to A17	Address Input pins
27 to 23, 22 to 18		Select 262,144 words in FeRAM memory array by 18
		Address Input pins. When these address inputs are changed
		during /CE equals to "L" level, reading operation of data
		selected in the address after transition will start.
7 to 10, 13 to 16,	I/O0 to	Data Input/Output pins
29 to 32, 35 to 38	I/O15	These are 16 bits bidirectional pins for reading and writing.
6	/CE	Chip Enable Input pin
		In case the /CE equals to "L" level and /ZZ equals to "H" level,
		device is activated and enables to start memory access.
		In writing operation, input data from I/O pins are latched at
		the rising edge of /CE and written to FeRAM memory array.
17	/WE	Write Enable Input pin
		Writing operation starts at the falling edge of /WE.
		Input data from I/O pins are latched at the rising edge of /WE
		and written to FeRAM memory array.
41	/OE	Output Enable Input pin
		When the /OE is "L" level, valid data are output to data bus.
		When the /OE is "H" level, all I/O pins become high
		impedance (High-Z) state.
28	/ZZ	Sleep Mode Input pin
		When the /ZZ becomes to "L" level, device transits to the
		Sleep Mode.
		During reading and writing operation, /ZZ pin shall be hold
		"H" level.
40, 39	/UB, /LB	Lower/Upper byte Control Input pins
		In case /LB or /UB equals to "L" level, it enables
		reading/writing operation of I/O0 to I/O7 or I/O8 to I/O15
		respectively. In case /LB and /UB equal to "H" level, all I/O
		pins become High-Z state.
11, 33	VDD	Supply Voltage pins
		Connect all two pins to the power supply.
12, 34	VSS	Ground pins
		Connect all two pins to ground.

Note: Please refer to the timing diagram for functional description of each pin.

## ■ BLOCK DIAGRAM



### **■ FUNCTIONAL TRUTH TABLE**

Operation Mode	/CE	/WE	/OE	A0 to A1	A2 to A17	/ZZ	/UB,/LB
Sleep	×	×	×	×	×	L	×
Standby	Н	×	×	×	×	Н	×
Read(/CE Control)	$\downarrow$	Н	L	H or L	H or L	Н	×
Address Access Read	L	Н	L	H or L	↑ or ↓	Н	×
Write(/CE Control)*1	$\downarrow$	L	×	H or L	H or L	Н	×
Write(/WE Control)*1*2	L	<b>1</b>	×	H or L	H or L	Н	×
Address Access Write*1*3	L	$\downarrow$	×	H or L	↑ or ↓	Н	×
Pre-charge	<b>↑</b>	×	×	×	×	Н	×
Page Read	L	Н	L	↑ or ↓	H or L	Н	L
/UB,/LB Access Wright	L	L	Н	H or L	H or L	Н	$\downarrow$
Page Address Write	L	$\downarrow$	Н	↑ or ↓	H or L	Н	L

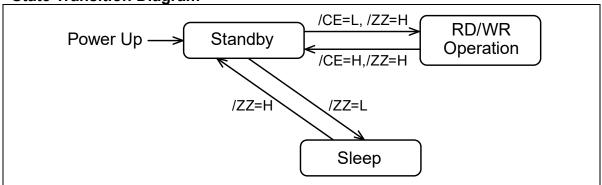
Note: H= "H" level, L= "L" level,  $\uparrow$ = Rising edge,  $\downarrow$ = Falling edge,  $\times$ = H, L,  $\downarrow$  or  $\uparrow$ 

<sup>\*1:</sup> In writing cycle, input data is latched at early rising edge of /CE or /WE.

<sup>\*2:</sup> In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.

<sup>\*3:</sup> In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

■ State Transition Diagram



## ■ FUNCTIONAL TRUTH TABLE OF BYTE CONTROL

Operation Mode	/WE	/OE	/LB	/UB	I/O0 to I/O7	I/O8 to I/O15
Dood(Without Output)	Н	Н	×	×	Hi-Z	Hi-Z
Read(Without Output)	Н	×	Н	Н	Hi-Z	Hi-Z
Read(I/O8 to I/O15)			Н	L	Hi-Z	Output
Read(I/O0 to I/O7)	Н	L	L	Н	Output	Hi-Z
Read(I/O0 to I/O15)			L	L	Output	Output
Write(I/O8 to I/O15)			Н	L	×	Input
Write(I/O0 to I/O7)	<b>1</b> ↑	×	L	Н	Input	×
Write(I/O0 to I/O15)			L	L	Input	Input

Note: H= "H" level, L= "L" level,  $\uparrow$ = Rising edge,  $\downarrow$ = Falling edge,  $\times$ = H, L,  $\downarrow$  or  $\uparrow$  Hi-Z= High Impedance

In case the byte reading or writing are not selected, /LB and /UB pins shall be connected to GND pin. In case the byte writing, while /CE=L, please don't switch /LB and /UB.

#### ■ ABABSOLUTE MAXIMUM RATINGS

Doromotor	Symbol	Rat	Heit	
Parameter	Symbol	Min	Max	Unit
Power Supply Voltage*	$V_{DD}$	- 0.5	+ 4.0	V
Input Pin Voltage*	$V_{\mathrm{IN}}$	- 0.5	$V_{DD} + 0.5 \ (\leq 4.0)$	V
Output Pin Voltage*	$V_{OUT}$	- 0.5	$V_{DD} + 0.5 \ (\leq 4.0)$	V
Operation Ambient Temperature	$T_{A}$	- 40	+ 105	°C
Storage Temperature	Tstg	- 55	+ 125	°C

<sup>\* :</sup> All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

### ■ RECOMMENDED OPERATING CONDITIONS

Doromotor	Cymbol		Value		Heit
Parameter	Symbol	Min	Тур	Max	Unit
Power Supply Voltage*1	$V_{ m DD}$	1.8	3.3	3.6	V
Operation Ambient Temperature*2	$T_A$	- 40	_	+ 105	°C

<sup>\*1:</sup> All voltages are referenced to VSS (ground 0 V).

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

<sup>\*2:</sup> Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

## **■ ELECTRICAL CHARACTERISTICS**

## 1. DC Characteristics

(within recommended operating conditions)

	0				alue	,	
Parameter	Sym -bol	Condition	Min	Тур	Max(TA ≤85°C)	Max(TA ≥ 85°C)	Unit
Input Leakage Current	$ I_{LI} $	$V_{IN} = 0V$ to $V_{DD}$	_	_	4	5	μΑ
Output Leakage Current	$ { m I}_{ m LO} $	$V_{OUT} = 0V$ to $V_{DD}$ /CE = $V_{IH}$ or /OE = $V_{IH}$	_	_		5	μΑ
Operating Power Supply Current*1	$I_{DD}$	$/CE = 0.2 \text{ V}, I_{out} = 0 \text{ mA}$	_	13.5	16	16	mA
Standby Current	$I_{SB}$	$\label{eq:ZZ} \begin{split} /ZZ \ge & V_{DD} - 0.2V \\ /CE, /WE, /OE \ge & V_{DD} - 0.2V \\ /LB, /UB \ge & V_{DD} - 0.2V \\ Others \ge & V_{DD} - 0.2V \text{ or } \le 0.2V \end{split}$	_	12	100	150	μΑ
Sleep Current	I <sub>ZZ</sub>	$\label{eq:ZZ = V_SS} $$ /CE, /WE, /OE \ge V_{DD} - 0.2V $$ /LB, /UB \ge V_{DD} - 0.2V $$ Others \ge V_{DD} - 0.2V $$ or \le 0.2V $$$	_	3.5	10	12	μΑ
High Level Input Voltage	$ m V_{IH}$	$V_{DD} = 1.8 V \text{ to } 3.6 V$	$V_{DD} \times 0.8$	_	$V_{DD}$	+ 0.3	V
Low Level Input Voltage	$V_{IL}$	$V_{DD} = 1.8 V \text{ to } 3.6 V$	- 0.3	_	$V_{DD}$	× 0.2	V
High Level	V <sub>OH1</sub>	$V_{DD} = 2.5V \text{ to } 3.6V$ $I_{OH} = -1.0\text{mA}$	$V_{DD} \times 0.8$	_	_	_	V
Output Voltage	V <sub>OH2</sub>	$V_{DD} = 1.8V \text{ to } 2.5V$ $I_{OH} = -100\mu\text{A}$	V <sub>DD</sub> - 0.2	_	_	_	v
Low Level	V <sub>OL1</sub>	$V_{DD} = 2.5V$ to 3.6V $I_{OL} = 2.0$ mA	_	_	0	.4	17
Output Voltage	$V_{OL2}$	$V_{DD} = 1.8V \text{ to } 2.5V$ $I_{OL} = 150 \mu A$	_	_	0	.2	V

<sup>\*1:</sup> During the measurement of I<sub>DD</sub>, all Address and I/O were taken to only change once per active cycle. Iout: output current

## 2. AC Characteristics

### AC Test Conditions

 $\begin{array}{ll} \mbox{Power Supply Voltage} & : 1.8 \ \mbox{V to } 3.6 \ \mbox{V} \\ \mbox{Operation Ambient Temperature} & : -40 \ \mbox{°C to } + 105 \ \mbox{°C} \\ \mbox{Input Voltage Amplitude} & : 0 \ \mbox{V / $V_{DD}$} \\ \end{array}$ 

 $\begin{array}{lll} \text{Input Voltage Amplitude} & : 0 \text{ V} / \text{V}_{\text{D}} \\ \text{Input Rising Time} & : 3 \text{ ns} \\ \text{Input Falling Time} & : 3 \text{ ns} \\ \text{Input Evaluation Level} & : \text{V}_{\text{DD}} / 2 \\ \text{Output Evaluation Level} & : \text{V}_{\text{DD}} / 2 \\ \text{Output Load Capacitance} & : 30 \text{ pF} \\ \end{array}$ 

## (1) Read Cycle

			TA≤+	· <b>85</b> °C		
Parameter	Symbol		alue	Valu	е	Unit
i didilietei	Symbol	(V <sub>DD</sub> =1.8	SV to 2.5V)	(V <sub>DD</sub> =2.5V 1	to 3.6V)	Oilit
		Min	Max	Min	Max	
Read Cycle time(/CE control)	$t_{ m RC}$	120	_	120	_	ns
Read Cycle time(Address access)	$t_{RCA}$	135	_	120	_	ns
/CE Access Time	$t_{\mathrm{CE}}$		65	_	65	ns
Address Access Time	$t_{AA}$		135	_	120	ns
/CE Output Data Hold time	$t_{\mathrm{OH}}$	0	_	0	_	ns
Address Access Output Data Hold	$t_{\mathrm{OAH}}$	20		20		ns
time	VOAH	20		20		115
/CE Active Time	$t_{\mathrm{CA}}$	65	_	65	_	ns
Pre-charge Time	$t_{\mathrm{PC}}$	55	_	55	_	ns
/LB, /UB Access Time	$t_{ m BA}$		35	_	20	ns
Address Setup Time	$t_{AS}$	0	_	0	_	ns
Address Hold Time	$t_{\mathrm{AH}}$	65	_	65	_	ns
/CE↑ to Address Transition time*1	tcah	0	_	0	_	ns
/OE Access Time	$t_{OE}$	_	35	_	20	ns
/CE Output Floating Time*1	$t_{ m HZ}$	1	10		10	ns
/OE Output Floating Time	t <sub>OHZ</sub>		10		10	ns
/LB, /UB Output Floating Time	$t_{ m BHZ}$		10		10	ns
Address Transition Time*1	$t_{AX}$	_	15	_	15	ns

<sup>\*1:</sup> Same parameters with the Write cycle.

			TA≥+	<b>85</b> °C		
Parameter	Symbol		alue	Valu		Unit
1 didilictor	Cymbol	(V <sub>DD</sub> =1.8	V to 2.5V)	(V <sub>DD</sub> =2.5V t	o 3.6V)	0
		Min	Max	Min	Max	
Read Cycle time(/CE control)	$t_{ m RC}$	125	_	125	_	ns
Read Cycle time(Address access)	$t_{RCA}$	140	_	125	_	ns
/CE Access Time	$t_{\rm CE}$	_	70		70	ns
Address Access Time	$t_{AA}$	l	140		125	ns
/CE Output Data Hold time	$t_{OH}$	0	_	0	_	ns
Address Access Output Data Hold	tour	20		20		ns
time	$t_{OAH}$	20	_	20		115
/CE Active Time	$t_{CA}$	70	_	70	_	ns
Pre-charge Time	$t_{\mathrm{PC}}$	55	_	55	_	ns
/LB, /UB Access Time	$t_{\mathrm{BA}}$		35		20	ns
Address Setup Time	$t_{AS}$	0	_	0	_	ns
Address Hold Time	$t_{AH}$	70	_	70	_	ns
/CE↑ to Address Transition time*1	tcah	0	_	0	_	ns
/OE Access Time	$t_{OE}$	_	35	_	20	ns
/CE Output Floating Time*1	$t_{\rm HZ}$		10		10	ns
/OE Output Floating Time	$t_{ m OHZ}$		10		10	ns
/LB, /UB Output Floating Time	$t_{ m BHZ}$		10		10	ns
Address Transition Time*1	$t_{AX}$	_	15	_	15	ns

<sup>\*1:</sup> Same parameters with the Write cycle.

(2) Write Cycle

1 Time Syste			TA≤+	<b>.85</b> °C		
Parameter	Symbol	Va	lue	Va	lue	Unit
Parameter	Symbol	(V <sub>DD</sub> =1.8)	V to 2.5V)	(V <sub>DD</sub> =2.5)	V to 3.6V)	Oilit
		Min	Max	Min	Max	
Write Cycle Time	$t_{ m WC}$	120	_	120	_	ns
/CE Active Time	$t_{CA}$	65	_	65	_	ns
/CE↓ to /WE↑ Time	$t_{\rm CW}$	65	_	65	_	ns
Pre-charge Time	$t_{\rm PC}$	55	_	55	_	ns
Write Pulse Width	$t_{\mathrm{WP}}$	20	_	20	_	ns
Address Setup Time	$t_{AS}$	0	_	0	_	ns
Address Hold Time	$t_{AH}$	65	_	65	_	ns
/WE↓ to /CE↑ Time	$t_{ m WLC}$	20	_	20	_	ns
(/UB or /LB) ↓ to /CE ↑	$t_{ m BLC}$	20	_	20	_	ns
Address Transition to /WE↑ Time	$t_{ m AWH}$	135	_	120	_	ns
/WE↑ to Address Transition Time	$t_{ m WHA}$	0	_	0	_	ns
Data Setup Time	$t_{ m DS}$	10	_	10	_	ns
Data Hold Time	$t_{\mathrm{DH}}$	0	_	0	_	ns
/WE Output Floating Time	$t_{\mathrm{WZ}}$	_	10	_	10	ns
/WE Output Access Time*1	$t_{\mathrm{WX}}$	10	_	10	_	ns
Write Setup Time*1	$t_{\mathrm{WS}}$	0	_	0	_	ns
Write Hold Time*1	$t_{ m WH}$	0	_	0	_	ns
/CE Output Floating Time	$t_{\rm HZ}$	_	10	_	10	ns
Address transition Time	$t_{AX}$		15	_	15	ns
/UB, /LB Write Pulse Width	$t_{\mathrm{WP2}}$	20	_	20	—	ns
/WE=L to (/UB, /LB)=H period	$t_{\mathrm{WP3}}$	20		20		ns

			TA≥+	<b>85</b> °C		
Parameter	Symbol		lue		lue	Unit
- Tarameter	Cymbol	(V <sub>DD</sub> =1.8)	√ to 2.5V)	(V <sub>DD</sub> =2.5)	V to 3.6V)	0
		Min	Max	Min	Max	
Write Cycle Time	$t_{ m WC}$	125	_	125		ns
/CE Active Time	$t_{CA}$	70	_	70		ns
/CE↓ to /WE↑ Time	$t_{\rm CW}$	70	_	70		ns
Pre-charge Time	$t_{PC}$	55	_	55		ns
Write Pulse Width	$t_{\mathrm{WP}}$	20	_	20		ns
Address Setup Time	$t_{AS}$	0	_	0		ns
Address Hold Time	$t_{\mathrm{AH}}$	70	_	70		ns
/WE↓ to /CE↑ Time	$t_{ m WLC}$	20	_	20		ns
(/UB or /LB) ↓ to /CE ↑	$t_{\rm BLC}$	20	_	20	_	ns
Address Transition to /WE↑ Time	$t_{ m AWH}$	140	_	125		ns
/WE↑ to Address Transition Time	$t_{ m WHA}$	0	_	0		ns
Data Setup Time	$t_{ m DS}$	10	_	10		ns
Data Hold Time	$t_{ m DH}$	0	_	0		ns
/WE Output Floating Time	$t_{ m WZ}$		10	_	10	ns
/WE Output Access Time*1	$t_{ m WX}$	10	_	10		ns
Write Setup Time*1	$t_{ m WS}$	0	_	0		ns
Write Hold Time*1	$t_{ m WH}$	0	_	0		ns
/CE Output Floating Time	$t_{\rm HZ}$		10		10	ns
Address transition Time	$t_{AX}$	_	15		15	ns
/UB, /LB Write Pulse Width	$t_{\mathrm{WP2}}$	20	_	20		ns
/WE=L to (/UB, /LB)=H period	$t_{\mathrm{WP3}}$	20	_	20	_	ns

(3) Page Mode Read/Write Cycle

Parameter	Symbol	Value (V <sub>DD</sub> =1.8V to 2.5V)		Value (V <sub>DD</sub> =2.5V to 3.6V)		Unit
		Min	Max	Min	Max	
Page Mode Write Cycle Time	$t_{\mathrm{PWC}}$	25	_	25	_	ns
Page Mode Write Pulse Width	$t_{\mathrm{WPP}}$	15	_	15	_	ns
Page Address Setup Time (/WE=L)	$t_{ASP}$	8	_	8	_	ns
Page Address Hold Time (/WE=L)	$t_{AHP}$	15	_	15	_	ns
Page Address Access Time	$t_{AAP}$		25	_	25	ns
Page Address Data Hold Time	$t_{\mathrm{OHP}}$	3	_	3	_	ns
Page Mode Read Cycle Time	$t_{\mathrm{PRCA}}$	25	_	25	_	ns
Page Mode Write Pre Charge Width	$t_{\mathrm{WPHP}}$	7	_	7	_	ns

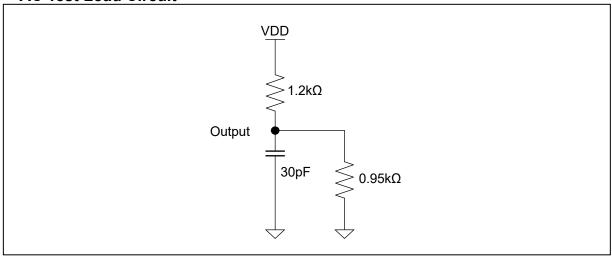
(4) Power ON/OFF Sequence and Sleep Mode Cycle

Doromotor	Cumbal	Va	Unit	
Parameter	Symbol	Min	Max	Unit
/CE level hold time for Power ON	$t_{ m PU}$	450	_	μs
/CE level hold time for Power OFF	$t_{\mathrm{PD}}$	85	_	ns
Power supply rising time	$t_{ m VR}$	50	_	μs/V
Power supply falling time	$t_{ m VF}$	100	_	μs/V
/ZZ active time	t <sub>ZZL</sub>	1	_	μs
Sleep mode enable time	t <sub>ZZEN</sub>	_	0	μs
/CE level hold time for Sleep mode release	t <sub>ZZEX</sub>	450	_	μs

3. Pin Capacitance

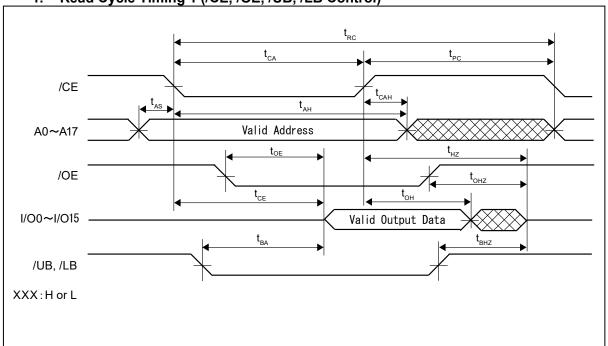
Parameter	Symbol	Condition	Value			Unit
Parameter	Symbol		Min	Тур	Max	Ullit
Input Capacitance	$C_{IN}$	N 22N	_	_	6	рF
Input/Output Capacitance (I/O pin)	$C_{I/O}$	$V_{DD} = 3.3 \text{ V},$ $f = 1 \text{ MHz}, T_A = +25 ^{\circ}\text{C}$	_	_	8	pF
/ZZ Pin Input Capacitance	$C_{ZZ}$	$1-1 \text{ MHz}, 1_A-+23 \text{ C}$	_	_	8	рF

## ■ AC Test Load Circuit

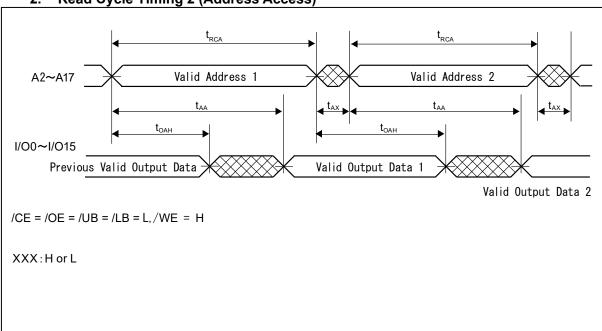


## **■ TIMING DIAGRAMS**

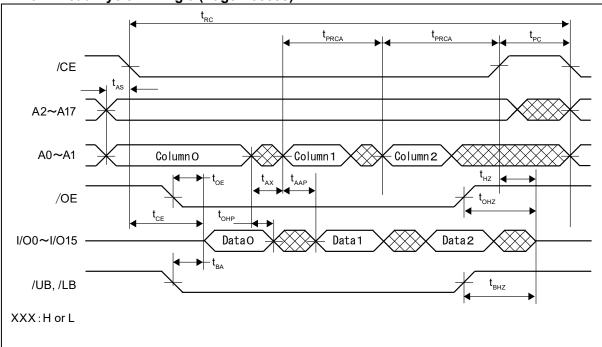
1. Read Cycle Timing 1 (/CE, /OE, /UB, /LB Control)



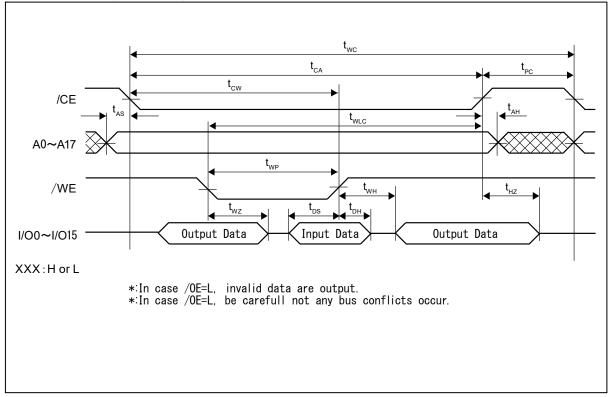
2. Read Cycle Timing 2 (Address Access)



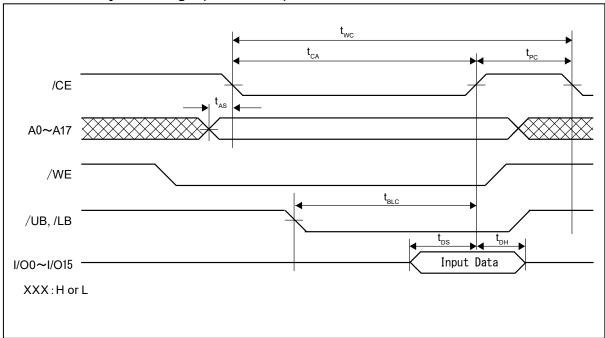




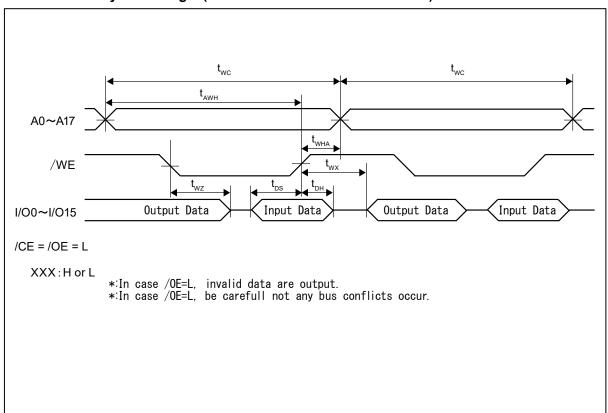
## 4. Write Cycle Timing 1 (/WE Control)



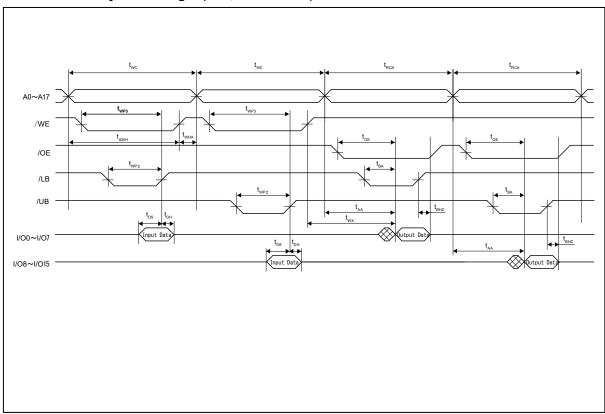
## 5. Write Cycle Timing 2 (/CE Control)



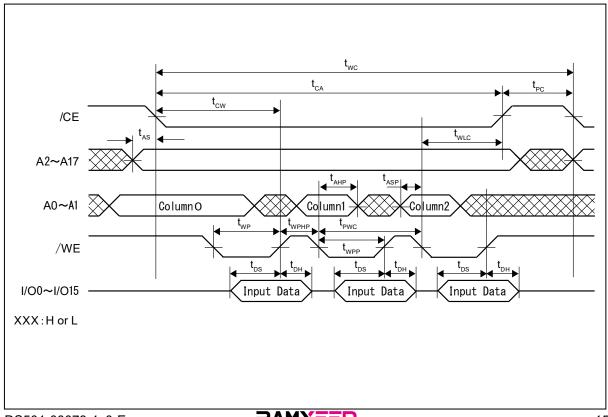
## 6. Write Cycle Timing 3 (Address Access and /WE Control)



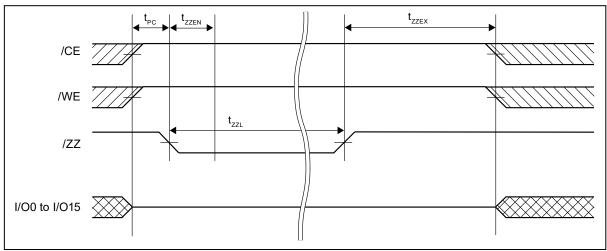
## 7. Write Cycle Timing 4 (/UB,/LB Access)



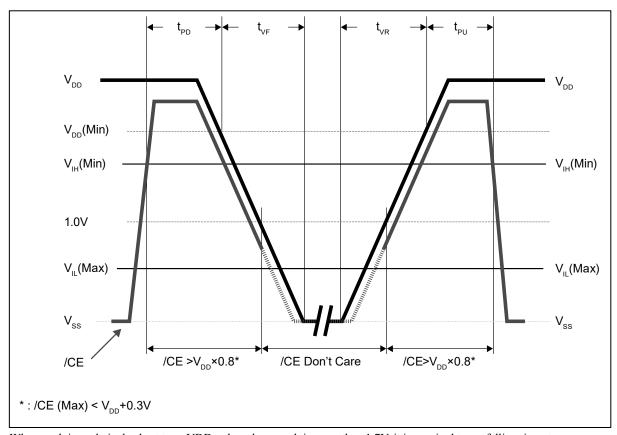
## Write Cycle Timing 5 (Page Address Access)



## 9. Sleep Mode Timing



## **■ POWER ON/OFF SEQUENCE**



When applying relatively short term VDD pulse whose peak is more than 1.7V, it is required to set falling time,  $t_{VF}$  more than 0.4ms/V. (In case VDD rises over 1.7V and falls just after that, if this term is short, device may lose its function.)

## **■ FeRAM CHARACTERISTICS**

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	$10^{13}$	_	Times/64bits	Operation Ambient Temperature $T_A = +105  ^{\circ}\text{C}$
	$10^{14}$	_		Operation Ambient Temperature $T_A = +85  ^{\circ}\text{C}$
Data Retention*2	10	_		Operation Ambient Temperature $T_A = +105  ^{\circ}\text{C}$
	40		Years	Operation Ambient Temperature $T_A = +85  ^{\circ}\text{C}$
	95	_		Operation Ambient Temperature $T_A = +55  ^{\circ}\text{C}$
	≥ 200	_		Operation Ambient Temperature $T_A = +35 ^{\circ}\text{C}$

<sup>\*1:</sup> Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

#### ■ NOTE ON USE

• We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

<sup>\*2:</sup> Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

## ■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant		≥  2000 V
ESD CDM (Charged Device Model) JESD22-C101 compliant	MS85R4M2TAFN-G-JAE2	≥  1000 V
Latch-Up (C-V Method) Proprietary method		≥  200 V

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

## ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

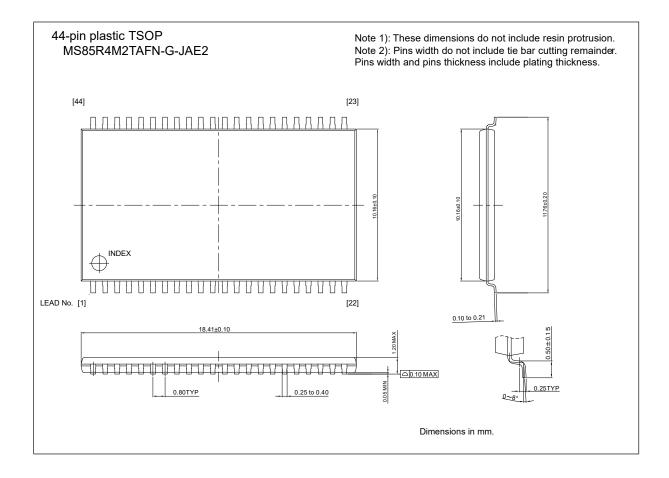
## ■ ORDERING INFORMATION

Part Number	Package	Shipping form	Minimum shipping quantity
MS85R4M2TAFN-G-JAE2	44-pin plastic TSOP	Tray	*

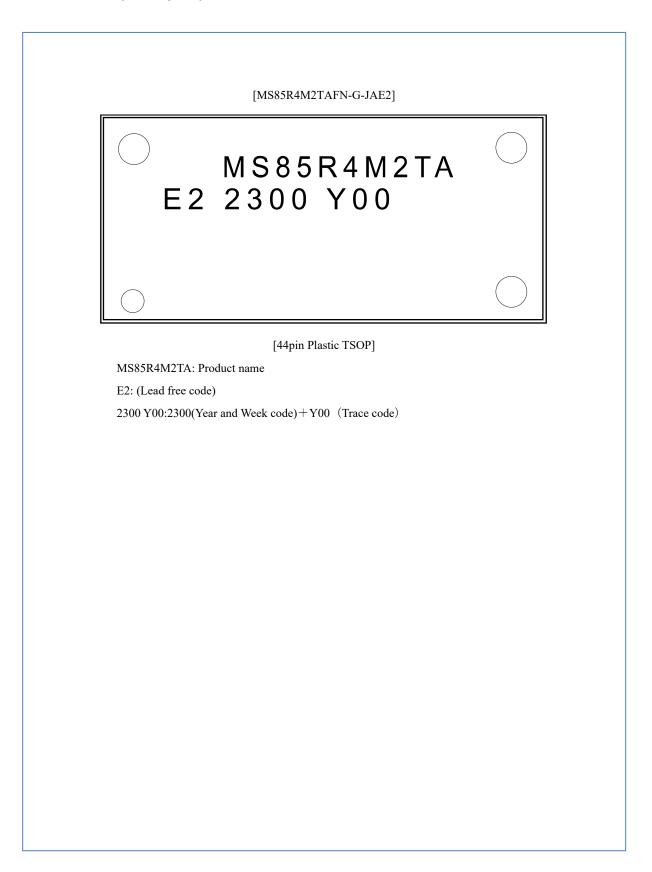
<sup>\*:</sup> Please contact our sales office about minimum shipping quantity.

## **■ PACKAGE DIMENSIONS**

44-pin plastic TSOP	Lead pitch	0.8mm
	Package width × package length	10.16 × 18.41mm
	Lead shape	Gullwing
THE REPORT	Sealing method	Plastic mold
THE RELEASE OF THE PARTY OF THE	Mounting height	1.2mm (max.)
Path the things		
MS85R4M2TAFN-G-JAE2		



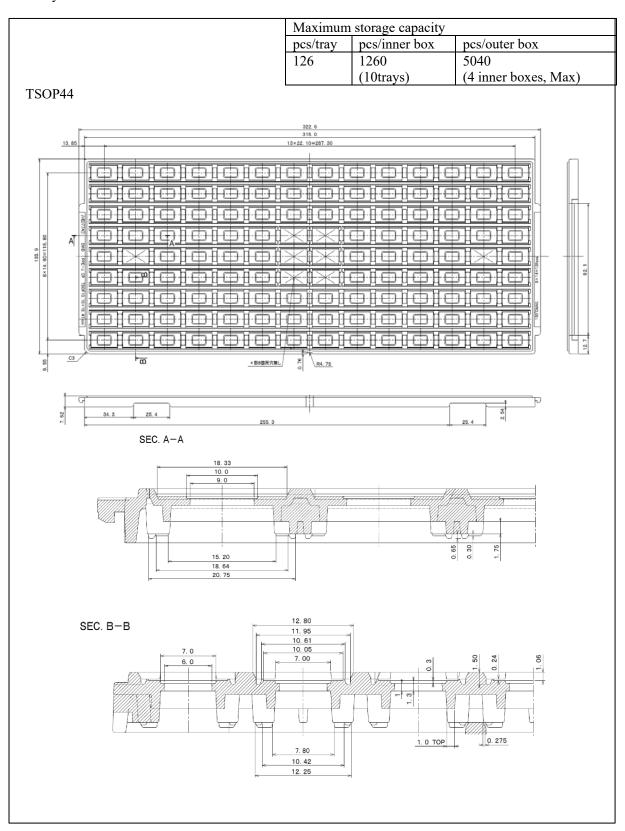
## ■ MARKING(Examples)



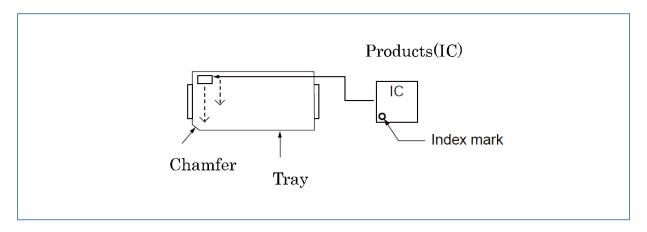
### **■ PACKING**

### MS85R4M2TAFN-G-JAE2

### 1.1 Tray dimensions

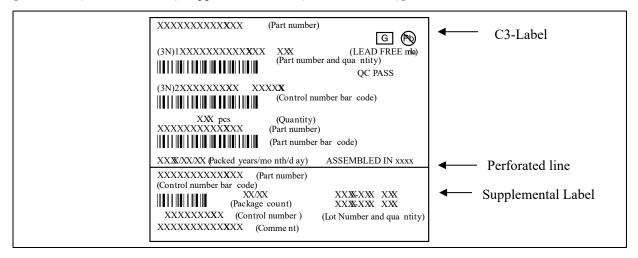


#### 1.2 IC orientation



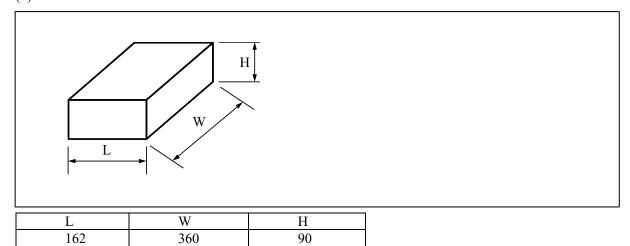
#### 1.3 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping) [C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



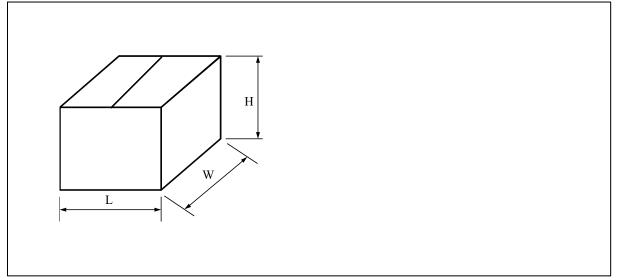
## 1.4 Dimensions for container

## (1) Dimensions for inner box



(Dimensions in mm)

## (2) Dimensions for outer box



L	W	Н
410	375	225

(Dimensions in mm)

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
_	Overall	Following technical word is revised to more commonly used one. FRAM to FeRAM

## RAMXEED LIMITED

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