RAMXEED

DS501-00096-1v0-E

Memory FeRAM

1M (128K × 8) Bit SPI

MS85RS1MTY(AEC-Q100 Compliant)

■ DESCRIPTION

MS85RS1MTY is a FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 131,072 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. This product is specifically targeted for high-temperature environment such as automobile applications.
MS85RS1MTY adopts the Serial Peripheral Interface (SPI).
The MS85RS1MTY is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MS85RS1MTY can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^{2}PROM.
As MS85RS1MTY does not need any waiting time in writing process, the write cycle time of MS85RS1MTY is much shorter than that of Flash memories or E^{2}PROM.

■ FEATURES

• Bit configuration	: 131,072 words × 8 bits
• Special Sector Region	: 256 words × 8 bits In this region, data storage after (by) three times reflow based on JEDEC MSL-3 standard condition is guaranteed.
• Unique ID	
• Serial Number	: 64 bits In this region, data storage after (by) three times reflow based on JEDEC MSL-3 standard condition is guaranteed.
• Serial Peripheral Interface	: SPI (Serial Peripheral Interfaces) Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
• Operating frequency	: 50 MHz (Max)
• High endurance	: 10^{13} times (+125 °C),
• Data retention	: 70.4 years (+85 °C), 19.1 years (+105 °C), 5.9 years (+125 °C) or more Under evaluation for more than 5.9 years(+125 °C)
• Operating power supply voltage	: 1.8 V to 3.6 V
• Low power consumption	: Operating power supply current 4mA (Max@50 MHz) Standby current 150µA (Max) Deep Power Down current 30µA (Max) Hibernate current 10µA (Max)
• Operation ambient temperature range	: – 40 °C to +125 °C
• Package	8-pin plastic SOP (150mil) 8-pin plastic DFN (5mm x 6mm) RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

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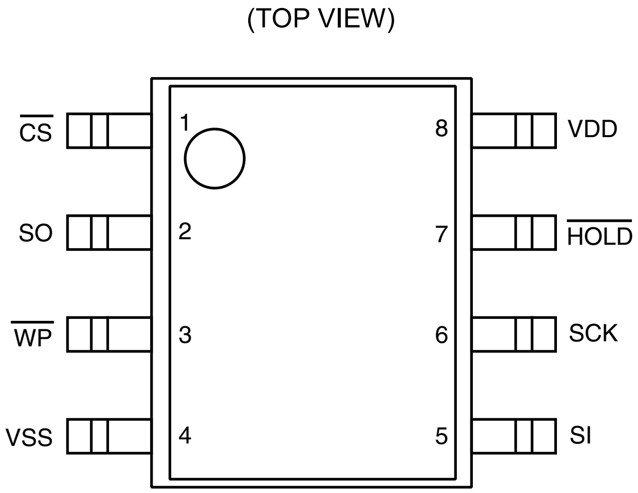
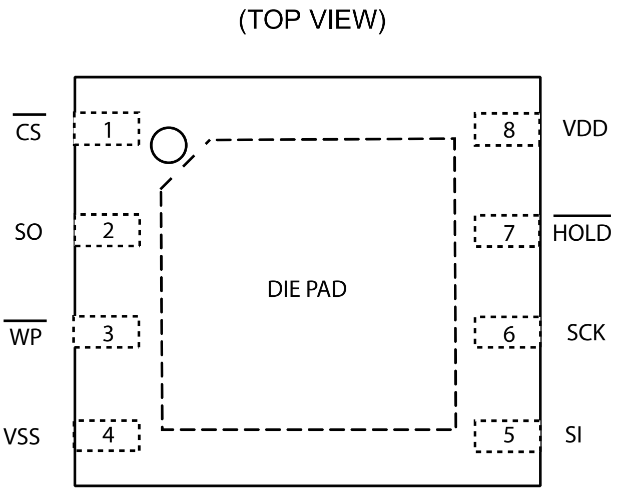
■ PIN ASSIGNMENT


(TOP VIEW)
$\overline{\text{CS}}$
SO
$\overline{\text{WP}}$
VSS
1
2
3
4
8
7
6
5
VDD
$\overline{\text{HOLD}}$
SCK
SI

8-pin plastic SOP(150mil)

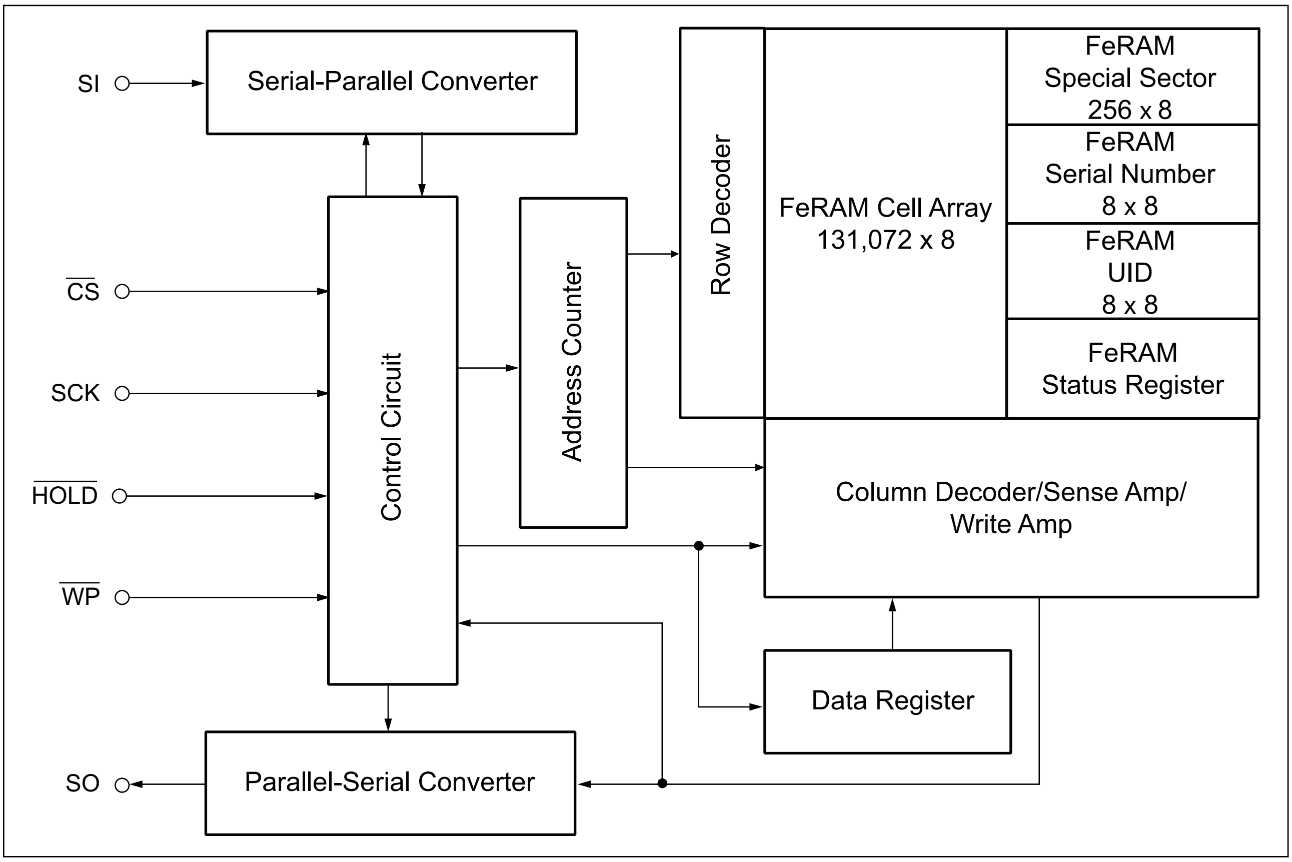

(TOP VIEW)
$\overline{\text{CS}}$
SO
$\overline{\text{WP}}$
VSS
1
2
3
4
8
7
6
5
DIE PAD
VDD
$\overline{\text{HOLD}}$
SCK
SI

8-pin plastic DFN(5mm x 6mm)

■ PIN FUNCTIONAL DESCRIPTIONS

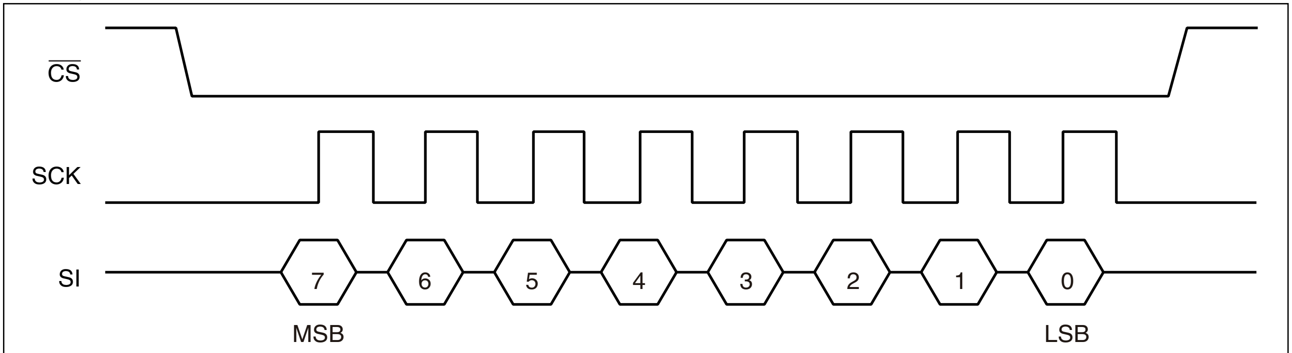
Pin No.	Pin Name	Functional description
1	$\overline{\text{CS}}$	Chip Select pin This is an input pin to make chips select. When $\overline{\text{CS}}$ is “H” level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{\text{CS}}$ is “L” level, device is in select (active) status. $\overline{\text{CS}}$ has to be “L” level before inputting op-code.
3	$\overline{\text{WP}}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see “■ STATUS REGISTER”) is protected in related with $\overline{\text{WP}}$ and WPEN. See “ ■WRITING PROTECT” for detail.
7	$\overline{\text{HOLD}}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{\text{HOLD}}$ is “L” level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. See “ ■HOLD OPERATION” for detail. The Hold pin is pulled up internally to the VDD pin.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FeRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin

■ BLOCK DIAGRAM

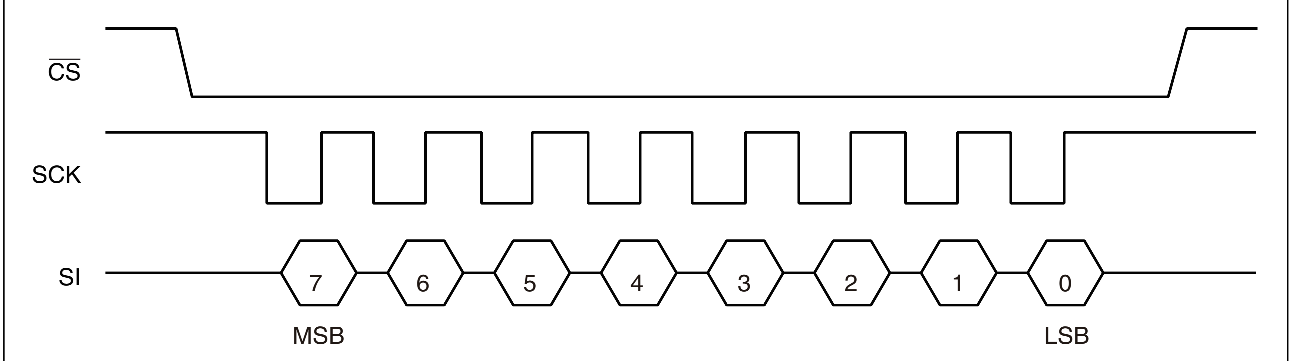

SI
CS
SCK
HOLD
WP
SO
Serial-Parallel Converter
Control Circuit
Address Counter
Row Decoder
FeRAM Cell Array
131,072 x 8
FeRAM
Special Sector
256 x 8
FeRAM
Serial Number
8 x 8
FeRAM
UID
8 x 8
FeRAM
Status Register
Column Decoder/Sense Amp/
Write Amp
Data Register
Parallel-Serial Converter

■ SPI MODE

MS85RS1MTY corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .


CS
SCK
SI
7
6
5
4
3
2
1
0
MSB
LSB

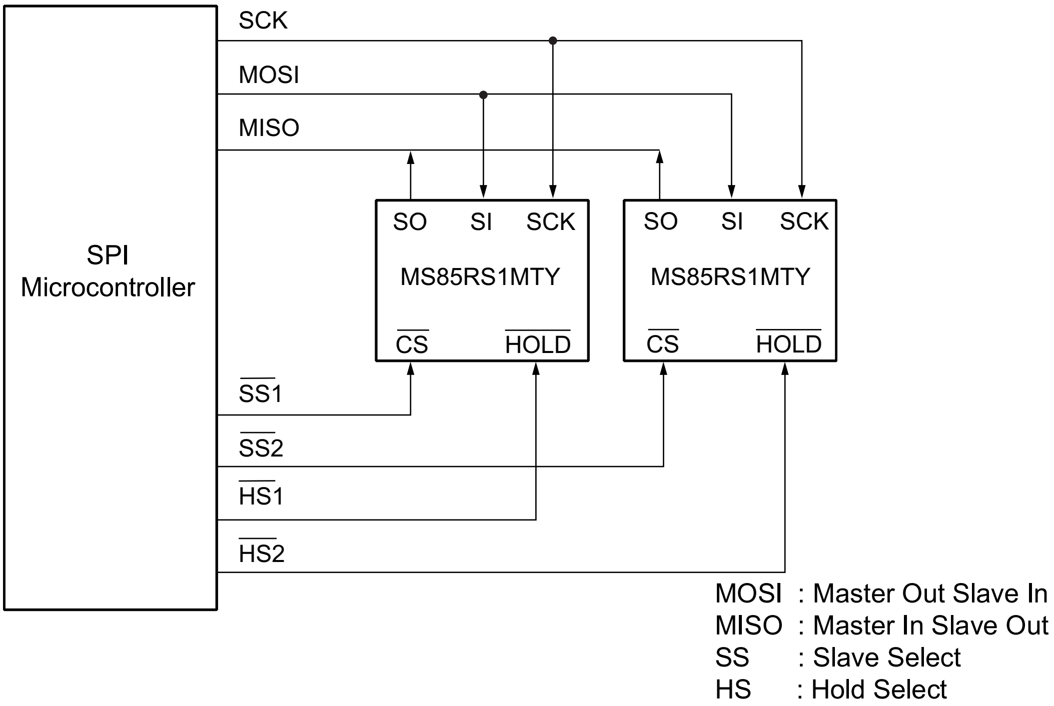
SPI Mode 0


CS
SCK
SI
7
6
5
4
3
2
1
0
MSB
LSB

SPI Mode 3

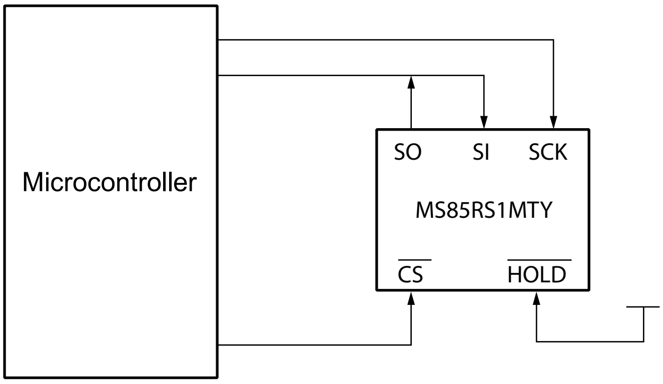
■ SERIAL PERIPHERAL INTERFACE (SPI)

MS85RS1MTY works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.


SCK
MOSI
MISO
SPI Microcontroller
SO SI SCK
MS85RS1MTY
$\overline{\text{CS}}$ $\overline{\text{HOLD}}$
SO SI SCK
MS85RS1MTY
$\overline{\text{CS}}$ $\overline{\text{HOLD}}$
$\overline{\text{SS1}}$
$\overline{\text{SS2}}$
$\overline{\text{HS1}}$
$\overline{\text{HS2}}$

MOSI : Master Out Slave In
MISO : Master In Slave Out
SS : Slave Select
HS : Hold Select

System Configuration with SPI Port


Microcontroller
SO SI SCK
MS85RS1MTY
$\overline{\text{CS}}$ $\overline{\text{HOLD}}$

System Configuration without SPI Port

■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FeRAM). WPEN protects writing to a status register (refer to "■ WRITING PROTECT") relating with $\overline{\text{WP}}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FeRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. After return from DPD mode. After return from Hibernate mode. Achieving continuous writing mode, WEL is not reset after following operations making it possible to execute writing commands continuously. After WRSR command recognition. After WRITE command recognition. After WRSN command recognition. After SSWR command recognition.
0	0	This is a bit fixed to "0".

■ OP-CODE

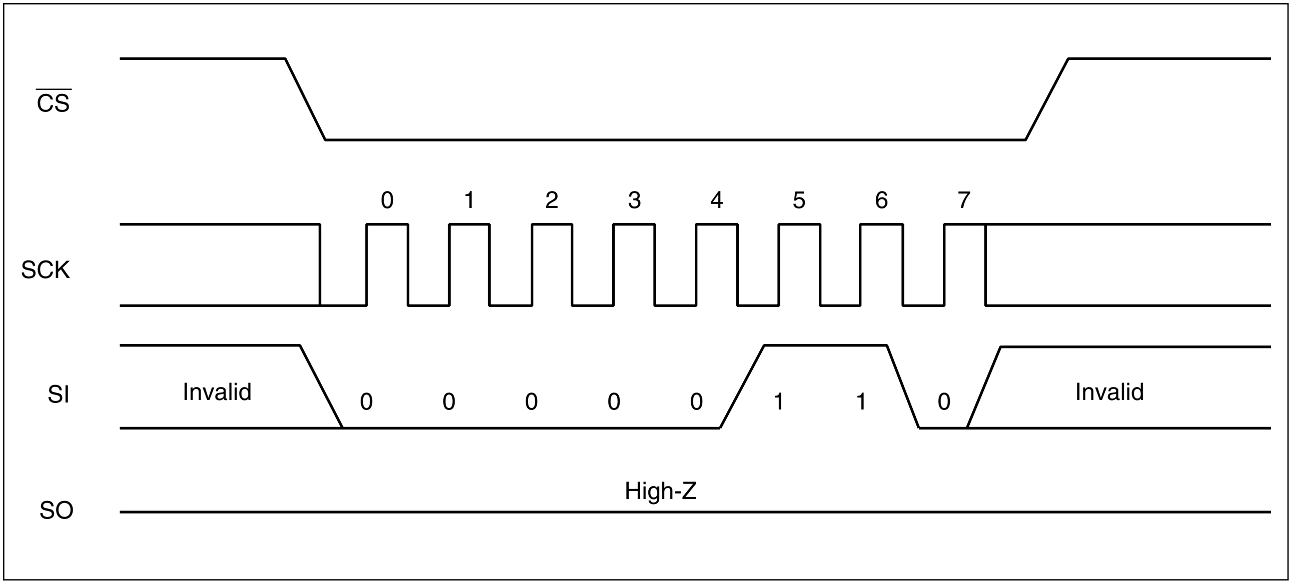
MS85RS1MTY accepts 16 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{CS}$ is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	$0000\ 0110_B$
WRDI	Reset Write Enable Latch	$0000\ 0100_B$
RDSR	Read Status Register	$0000\ 0101_B$
WRSR	Write Status Register	$0000\ 0001_B$
READ	Read Memory Code	$0000\ 0011_B$
WRITE	Write Memory Code	$0000\ 0010_B$
FSTRD	Fast Read Memory Code	$0000\ 1011_B$
DPD	Deep Power Down Mode	$1011\ 1010_B$
HIBERNATE	Hibernate Mode	$1011\ 1001_B$
RDID	Read Device ID	$1001\ 1111_B$
RUID	Read Unique ID	$0100\ 1100_B$
WRSN	Write Serial Number	$1100\ 0010_B$
RDSN	Read Serial Number	$1100\ 0011_B$
SSWR	Write Special Sector	$0100\ 0010_B$
SSRD	Read Special Sector	$0100\ 1011_B$
FSSRD	Fast Read Special Sector	$0100\ 1001_B$
RFU	Reserved	$1100\ 1110_B$
		$1100\ 1111_B$
		$1100\ 1100_B$

■ COMMAND

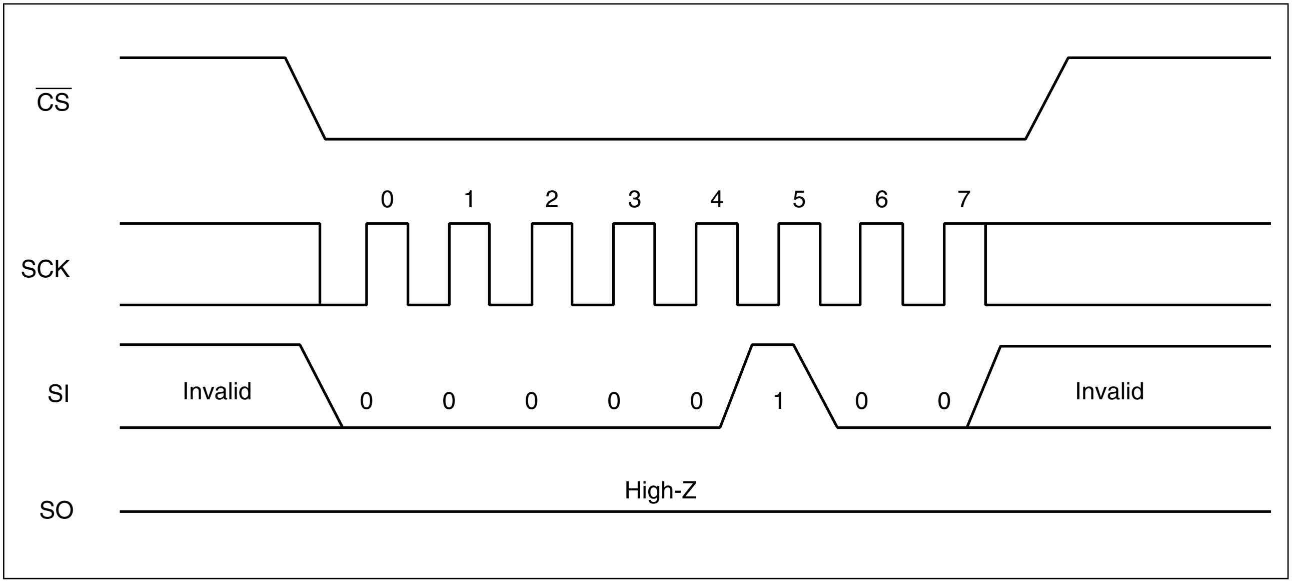
• WREN

The WREN command sets WEL (Write Enable Latch) bit to 1. WEL has to be set with the WREN command before writing operation (WRSR command, WRITE command, WRSN command and SSWR command) .


$\overline{CS}$
SCK
0 1 2 3 4 5 6 7
SI
Invalid
0 0 0 0 0 1 1 0
Invalid
SO
High-Z

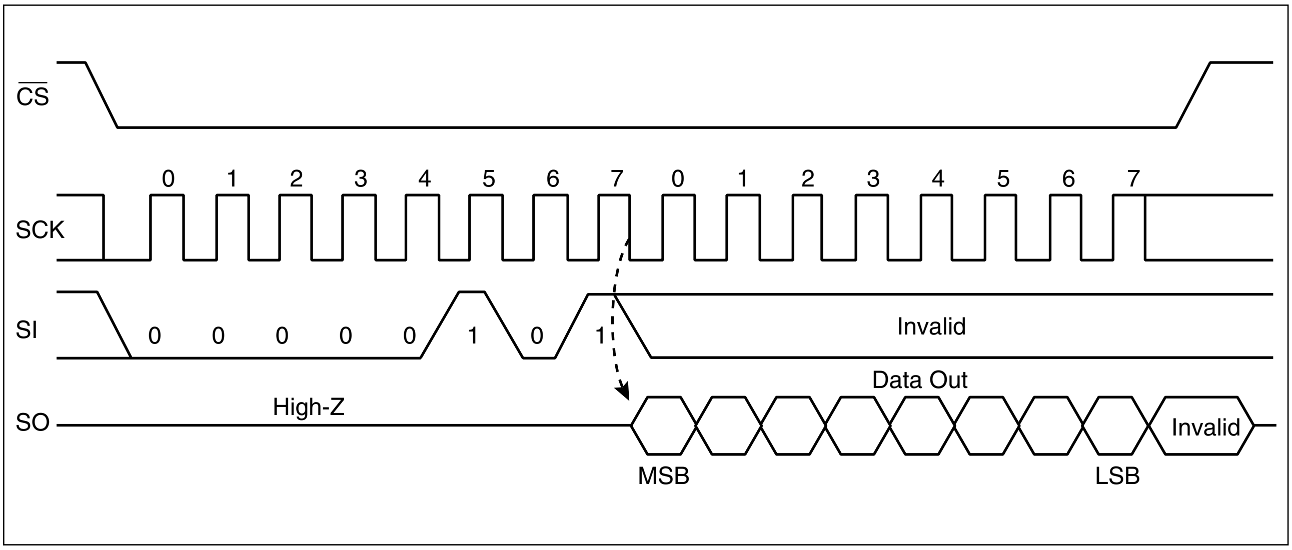
• WRDI

The WRDI command resets WEL (Write Enable Latch) bit to 0. Writing operation (WRSR command, WRITE command, WRSN command and SSWR command) are not performed when WEL is reset.


$\overline{CS}$
SCK
0 1 2 3 4 5 6 7
SI
Invalid
0 0 0 0 0 1 0 0
Invalid
SO
High-Z

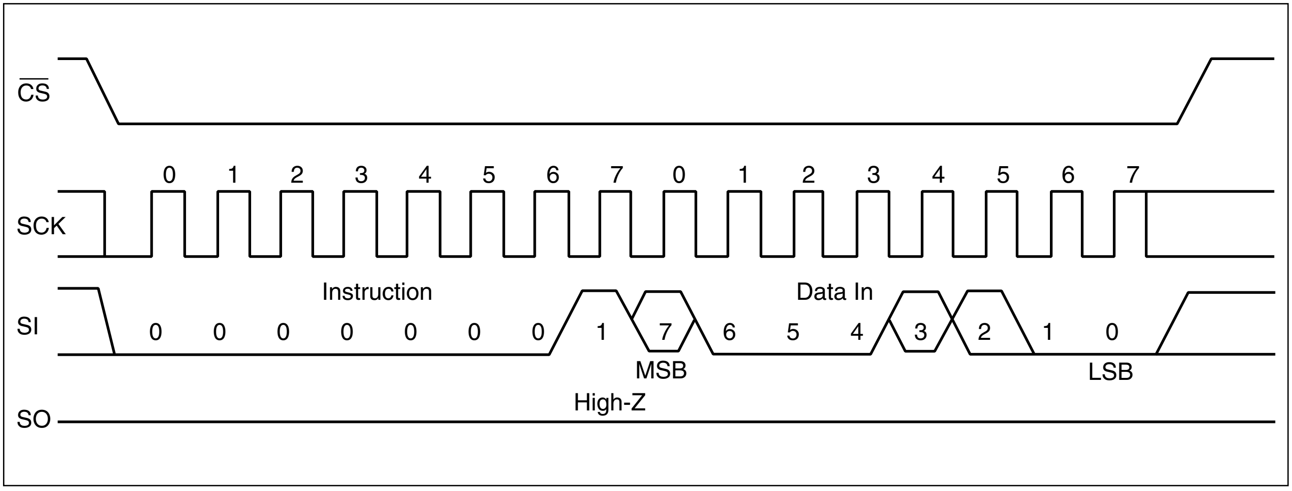
- **RDSR**

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{\text{CS}}$.


CS
SCK
SI
SO
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
0 0 0 0 0 1 0 1
Invalid
Data Out
High-Z
Invalid
MSB
LSB

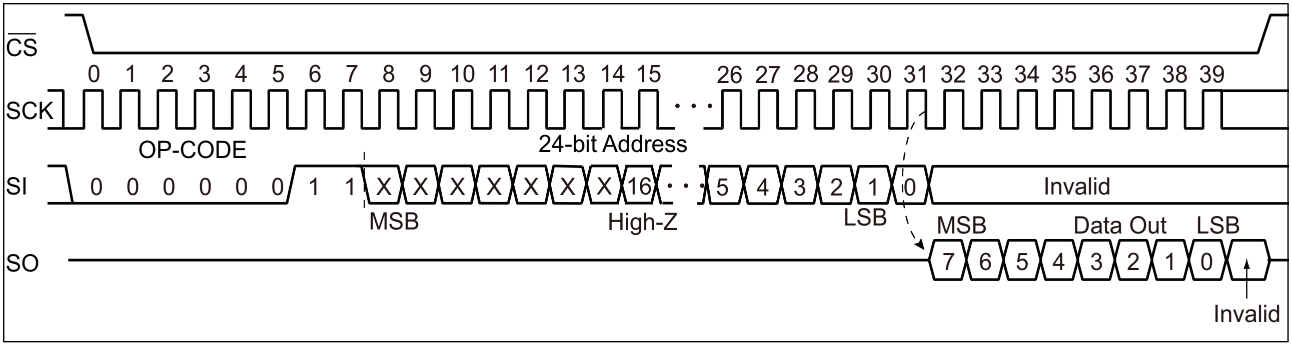
- **WRSR**

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to “0” and cannot be written. The SI value corresponding to bit 0 is ignored. $\overline{\text{WP}}$ signal level shall be fixed before performing WRSR command, and do not change the $\overline{\text{WP}}$ signal level until the end of command sequence.


CS
SCK
SI
SO
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
Instruction
Data In
0 0 0 0 0 0 0 1 7 6 5 4 3 2 1 0
MSB
LSB
High-Z

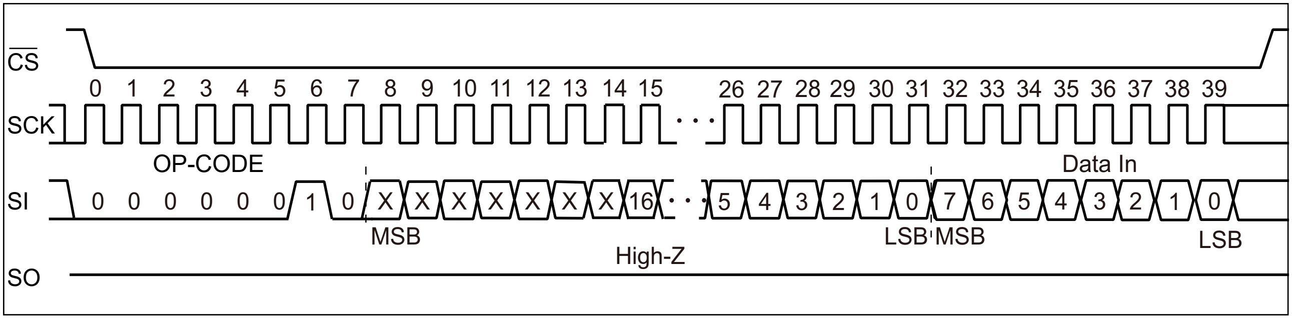
- **READ**

The READ command reads FeRAM memory cell array data. Arbitrary 24 bits address and op-code of READ are input to SI. The 7-bit upper address is invalid.Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When CS is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before CS rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
26 27 28 29 30 31 32 33 34 35 36 37 38 39
OP-CODE
24-bit Address
SI
0 0 0 0 0 0 1 1
X X X X X X X 16
5 4 3 2 1 0
Invalid
MSB
High-Z
LSB
MSB
Data Out
LSB
SO
7 6 5 4 3 2 1 0
Invalid

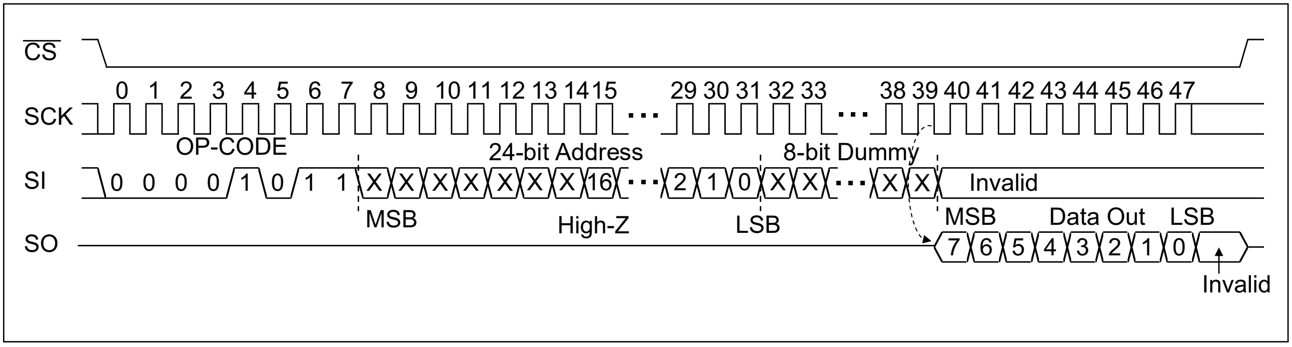
- **WRITE**

The WRITE command writes data to FeRAM memory cell array. WRITE op-code, arbitrary 24 bits of address and 8 bits of writing data are input to SI. The 7-bit upper address is invalid.When 8 bits of writing data is input, data is written to FeRAM memory cell array. Risen CS will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before CS rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely.


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
26 27 28 29 30 31 32 33 34 35 36 37 38 39
OP-CODE
Data In
SI
0 0 0 0 0 0 1 0
X X X X X X X 16
5 4 3 2 1 0
7 6 5 4 3 2 1 0
MSB
High-Z
LSB
MSB
LSB
SO

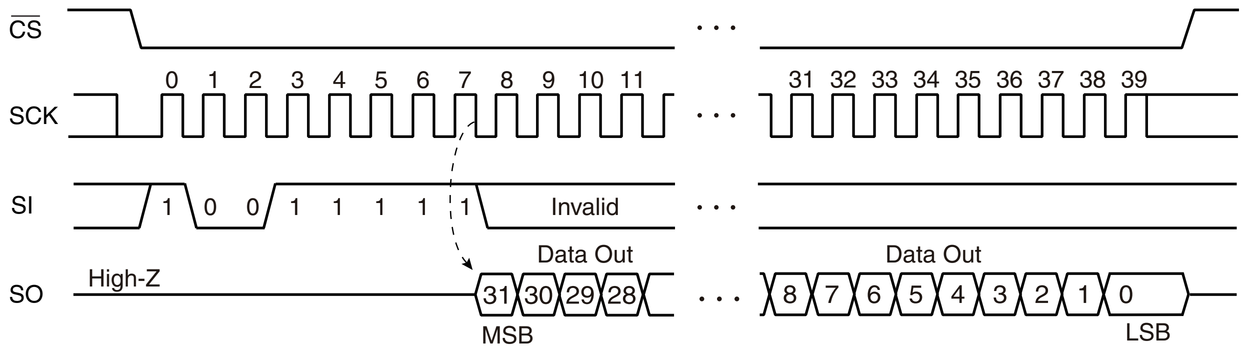
- **FSTRD**

The FSTRD command reads FeRAM memory cell array data. Arbitrary 24bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 7-bit upper address is invalid.Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When CS is risen, the FSTRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before CS rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
29 30 31 32 33
38 39 40 41 42 43 44 45 46 47
OP-CODE
24-bit Address
8-bit Dummy
SI
0 0 0 0 1 0 1 1
X X X X X X X 16
2 1 0
X X X X
Invalid
MSB
High-Z
LSB
MSB
Data Out
LSB
SO
7 6 5 4 3 2 1 0
Invalid

- **RDID**

The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, 32-bit Device ID is output by continuously sending SCK clock, and SO holds the output state of the last bit until $\overline{CS}$ is risen.


$\overline{CS}$
SCK
0 1 2 3 4 5 6 7 8 9 10 11
31 32 33 34 35 36 37 38 39
SI
1 0 0 1 1 1 1 1
Invalid
SO
High-Z
Data Out
31 30 29 28
MSB
Data Out
8 7 6 5 4 3 2 1 0
LSB

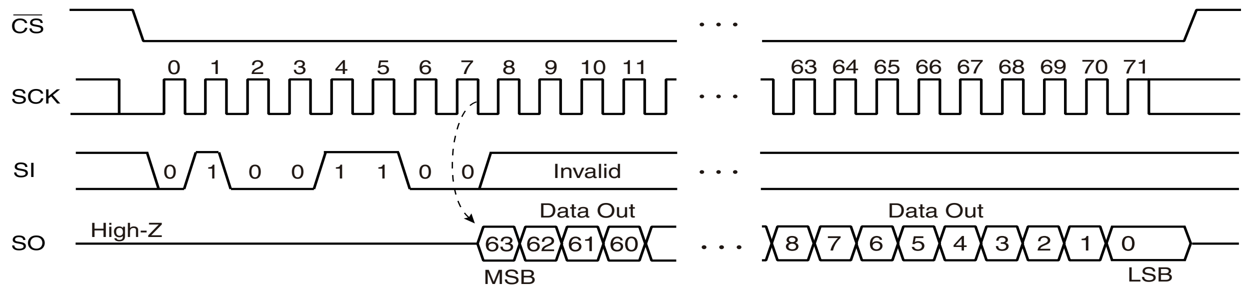
	bit									
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Hex**	
Manufacturer ID	0	0	0	0	0	1	0	0	04_H	Fujitsu
Continuation code	0	1	1	1	1	1	1	1	$7F_H$	

	Proprietary use			**Density**					**Hex**	
Product ID (1st Byte)	0	1	0	0	0	1	1	1	47_H	Density: 00111_B = 1Mbit

	Proprietary use								**Hex**	
Product ID (2nd Byte)	0	0	0	0	0	0	1	1	03_H	

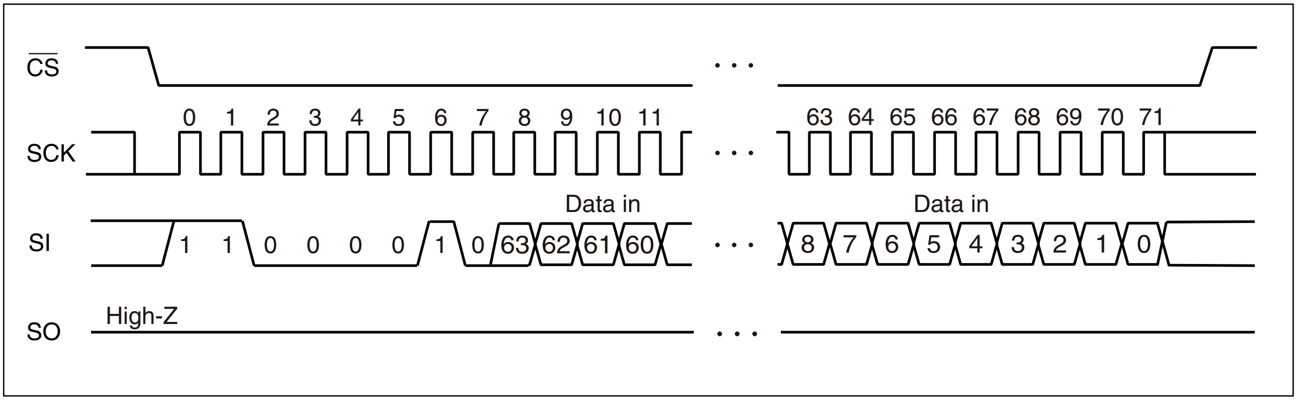
- RUID

The RUID command reads an unique ID which is defined in 64bits for each device. After performing RUID op-code to SI, 64-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK.
The unique ID is stable between before and after reflow. Refer "■ REFLOW CONDITIONS AND FLOOR LIFE" for the reflow condition.


$\overline{CS}$
SCK
0 1 2 3 4 5 6 7 8 9 10 11
63 64 65 66 67 68 69 70 71
SI
0 1 0 0 1 1 0 0
Invalid
SO
High-Z
Data Out
63 62 61 60
MSB
Data Out
8 7 6 5 4 3 2 1 0
LSB

- WRSN

The WRSN command writes data to serial number region which is allowed to write only one time. After performing WRSN op-code to SI, 64bits of writing data is input. Once wrote, the serial number region is protected, disabling to overwrite even when issuing WRSN command.
$\overline{\text{WP}}$ signal level shall be fixed before performing WRSN command, and do not change the $\overline{\text{WP}}$ signal level until the end of command sequence.

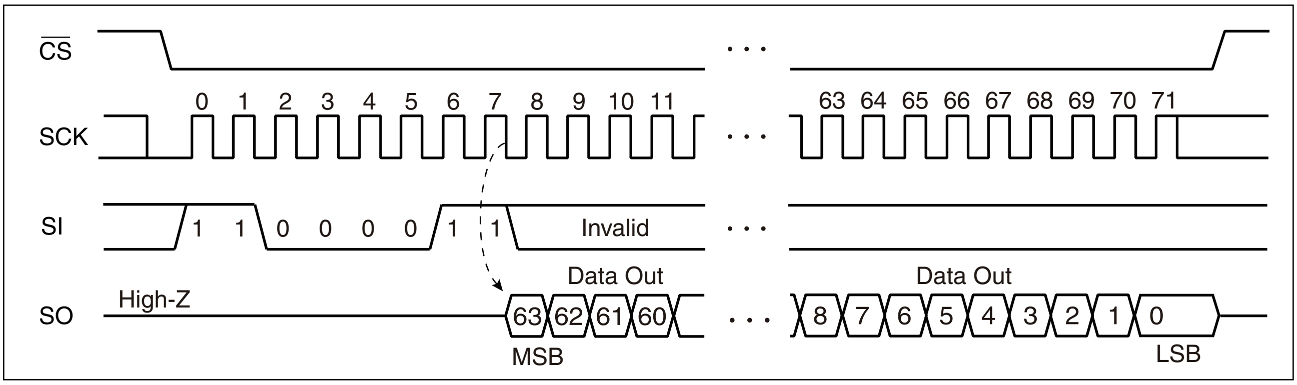


CS
SCK
SI
SO
0 1 2 3 4 5 6 7 8 9 10 11
63 64 65 66 67 68 69 70 71
Data in
1 1 0 0 0 0 1 0 63 62 61 60
Data in
8 7 6 5 4 3 2 1 0
High-Z

- RDSN

The RDSN command reads 64 bits of serial number which is written using WRSN command. After performing RDSN op-code to SI, 64-cycle clock to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. When reading serial number from devices which no WRSN command is executed, “0” for all bits are output.

The serial number is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.

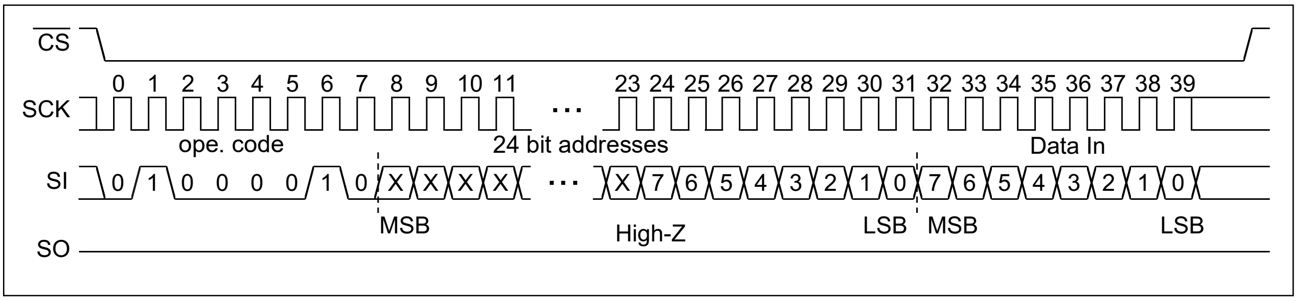


CS
SCK
SI
SO
0 1 2 3 4 5 6 7 8 9 10 11
63 64 65 66 67 68 69 70 71
1 1 0 0 0 0 1 1
Invalid
High-Z
Data Out
63 62 61 60
MSB
Data Out
8 7 6 5 4 3 2 1 0
LSB

- SSWR

The SSWR command writes data to special sector (a special region of 256 Byte in FeRAM). SSWR op-code, arbitrary 24 bits address and 8-bit writing data are input to SI. The 16-bit upper address is invalid. When input of 8-bit writing data is completed, it starts writing data to special sector. Risen $\overline{\text{CS}}$ will terminate the SSWR command, but if you continue the writing data for each before $\overline{\text{CS}}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, roll over is not happen, the data hereafter is ignored.

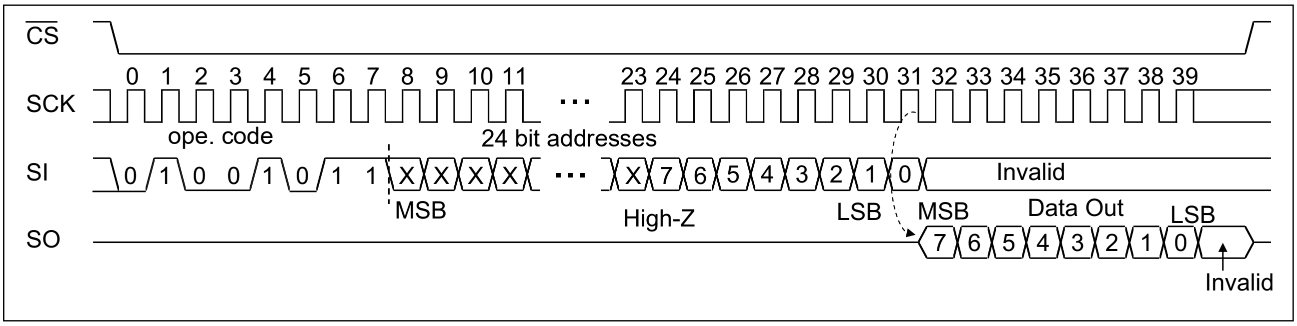
The data in special sector is stable between before and after reflow. Refer "■ REFLOW CONDITIONS AND FLOOR LIFE" for the reflow condition.


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11 ⋯ 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
ope. code
24 bit addresses
Data In
SI
0 1 0 0 0 0 1 0 X X X X ⋯ X 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0
MSB
High-Z
LSB
MSB
LSB
SO

- SSRD

The SSRD command reads data from special sector (a special region of 256 Byte in FeRAM). SSWR op-code and arbitrary 24 bits address are input to SI. The 16-bit upper address is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{\text{CS}}$ is risen, the SSRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{\text{CS}}$ rising. When it reaches the most significant address, roll over is not happen.

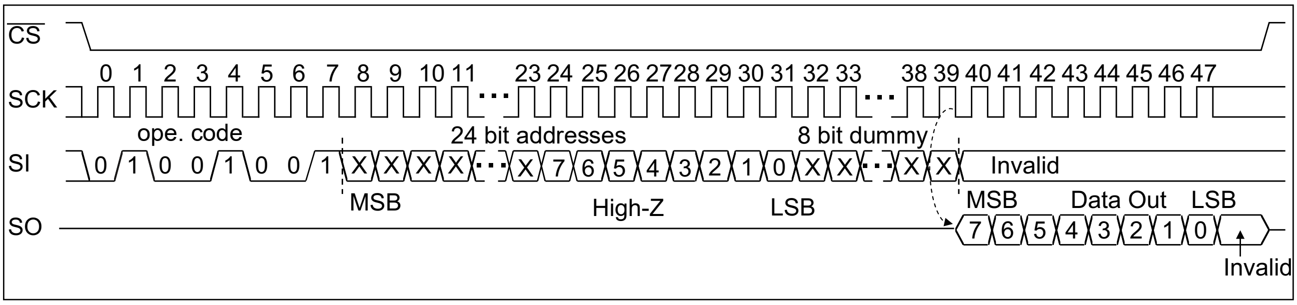
The data in special sector is stable between before and after reflow. Refer "■ REFLOW CONDITIONS AND FLOOR LIFE" for the reflow condition.


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11 ⋯ 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
ope. code
24 bit addresses
SI
0 1 0 0 1 0 1 1 X X X X ⋯ X 7 6 5 4 3 2 1 0
Invalid
MSB
High-Z
LSB
MSB
Data Out
LSB
SO
7 6 5 4 3 2 1 0
Invalid

- FSSRD

The SSRD command reads data from special sector (a special region of 256 Byte in FeRAM). SSWR op-code and arbitrary 24 bits address are input to SI followed by 8 bits dummy. The 7-bit upper address is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When CS is risen, the SSRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before CS rising. When it reaches the most significant address, roll over is not happen.

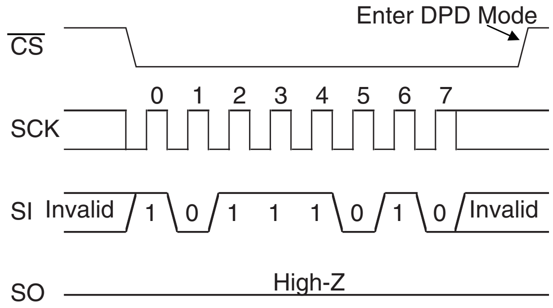
The data in special sector is stable between before and after reflow. Refer “■ REFLOW CONDITIONS AND FLOOR LIFE” for the reflow condition.


CS
SCK
SI
SO
0 1 2 3 4 5 6 7 8 9 10 11
23 24 25 26 27 28 29 30 31 32 33
38 39 40 41 42 43 44 45 46 47
ope. code
24 bit addresses
8 bit dummy
0 1 0 0 1 0 0 1
X X X X X 7 6 5 4 3 2 1 0 X X X X
Invalid
MSB
High-Z
LSB
MSB
Data Out
LSB
7 6 5 4 3 2 1 0
Invalid

- DPD(Deep Power Down)

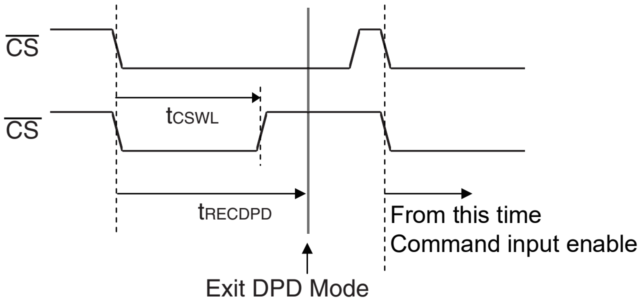
The DPD command shifts the LSI to a low power mode called “DPD mode”. The transition to the DPD mode is carried out at the rising edge of $\overline{CS}$ after operation code in the DPD command. However, when at least one SCK clock is inputted before the rising edge of $\overline{CS}$ after operation code in the DPD command, this DPD command is canceled.

After the DPD mode transition, SCK and SI inputs are ignored and SO changes to a High-Z state.


Enter DPD Mode
CS
0 1 2 3 4 5 6 7
SCK
SI Invalid 1 0 1 1 1 0 1 0 Invalid
SO
High-Z

DPD Mode Entry

Returning to an normal operation from the DPD mode is carried out after t_{RECDPD} (Max 10 μs) time from the falling edge of $\overline{CS}$ (see the figure below). It is possible to return $\overline{CS}$ to H level before t_{RECDPD} time. However, it is prohibited to bring down $\overline{CS}$ to L level again during t_{RECDPD} period.

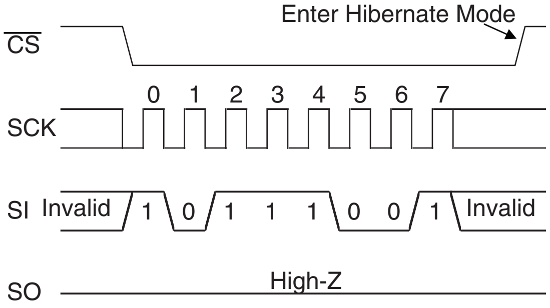

CS
CS
tCSWL
tRECDPD
From this time
Command input enable
Exit DPD Mode

DPD Mode Exit

- HIBERNATE

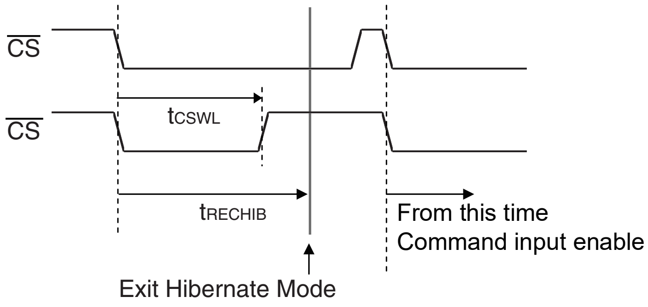
The HIBERNATE command shifts the LSI to a low power mode called “HIBERNATE mode”. The transition to the HIBERNATE mode is carried out at the rising edge of $\overline{CS}$ after operation code in the HIBERNATE command. However, when at least one SCK clock is inputted before the rising edge of $\overline{CS}$ after operation code in the HIBERNATE command, this HIBERNATE command is canceled.

After the HIBERNATE mode transition, SCK and SI inputs are ignored and SO changes to a High-Z state.


Enter Hibernate Mode
CS
0 1 2 3 4 5 6 7
SCK
SI Invalid 1 0 1 1 1 0 0 1 Invalid
SO
High-Z

Hibernate Mode Entry

Returning to an normal operation from the HIBERNATE mode is carried out after t_{RECHIB} (Max 450 µs) time from the falling edge of $\overline{CS}$ (see the figure below). It is possible to return $\overline{CS}$ to H level before t_{RECHIB} time. However, it is prohibited to bring down $\overline{CS}$ to L level again during t_{RECHIB} period.


CS
CS
tCSWL
tRECHIB
From this time
Command input enable
Exit Hibernate Mode

Hibernate Mode Exit

■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	18000_H to $1FFFF_H$ (upper 1/4)
1	0	10000_H to $1FFFF_H$ (upper 1/2)
1	1	00000_H to $1FFFF_H$ (all)

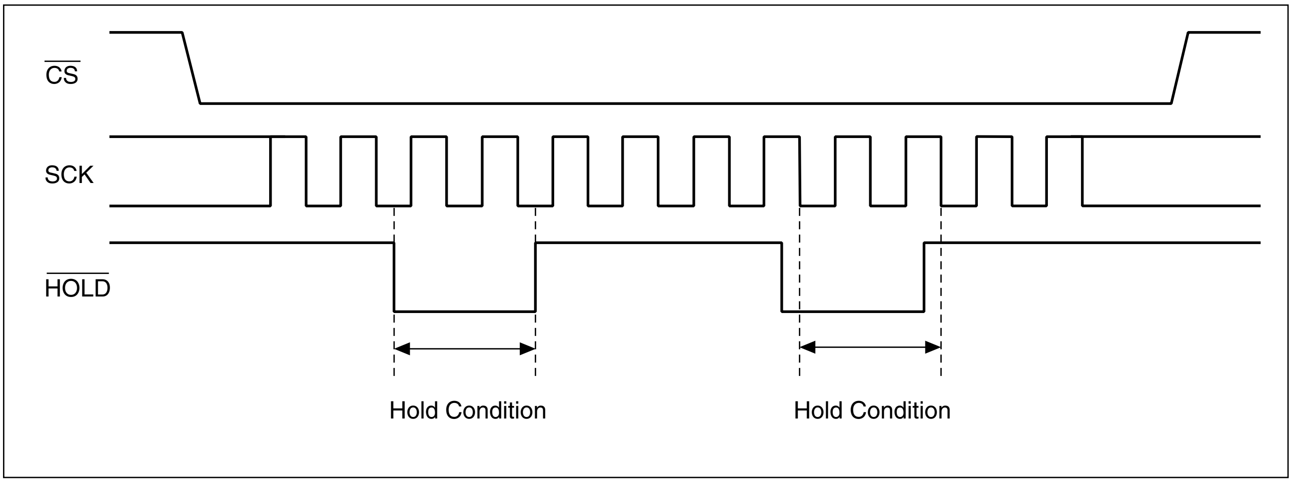
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, $\overline{\mathrm{WP}}$ as shown in the table.

WEL	WPEN	$\overline{\mathrm{WP}}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{\mathrm{HOLD}}$ is “L” level while $\overline{\mathrm{CS}}$ is “L” level. The timing for starting and ending hold status depends on the SCK to be “H” level or “L” level when a $\overline{\mathrm{HOLD}}$ pin input is transited to the hold condition as shown in the diagram below. In case the $\overline{\mathrm{HOLD}}$ pin transited to “L” level when SCK is “L” level, return the $\overline{\mathrm{HOLD}}$ pin to “H” level at SCK being “L” level. In the same manner, in case the $\overline{\mathrm{HOLD}}$ pin transited to “L” level when SCK is “H” level, return the $\overline{\mathrm{HOLD}}$ pin to “H” level at SCK being “H” level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If $\overline{\mathrm{CS}}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	– 0.5	+ 4.0	V
Input voltage*	V_{IN}	– 0.5	V_{DD} + 0.5(≤ 4.0)	V
Output voltage*	V_{OUT}	– 0.5	V_{DD} + 0.5(≤ 4.0)	V
Operation ambient temperature	T_A	– 40	+ 125	°C
Storage temperature	Tstg	– 55	+ 150	°C

*: These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage[*1]	V_{DD}	1.8	3.3	3.6	V
Operation ambient temperature[*2]	T_A	– 40	—	+ 125	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Sym-bol	Condition		Value			Unit
				Min	Typ (T_A=25 °C)	Max	
Input leakage current*1	$\|I_{LI}\|$	$\overline{\text{CS}}$ = V_{DD}	25 °C	—	—	1	μA
			125 °C	—	—	2	
		$\overline{\text{WP}}$, SCK,$\overline{\text{CS}}$ SI = 0 V to V_{DD}	25 °C	—	—	1	
			125 °C	—	—	2	
		HOLD = 0 V to V_{DD}	25 °C	—	—	100	
			125 °C	—	—	100	
Output leakage current*2	$\|I_{LO}\|$	SO = 0 V to V_{DD}	25 °C	—	—	1	μA
			125 °C	—	—	2	
Operating power supply current*3	I_{DD}	SCK = 50MHz		—	3	4	mA
Standby current	I_{SB}	SCK = SI = $\overline{\text{CS}}$ = $\overline{\text{WP}}$ = V_{DD}		—	12	150	μA
Hibernate current	I_{ZZHIB}	$\overline{\text{CS}}$ = V_{DD} All inputs V_{SS} or V_{DD}		—	0.3	10	μA
DPD current	I_{ZZDPD}	$\overline{\text{CS}}$ = V_{DD} All inputs V_{SS} or V_{DD}		—	6	30	μA
Input high voltage	V_{IH}	V_{DD} = 1.8 V to 3.6 V		$V_{DD} \times 0.8$	—	$V_{DD} + 0.5$	V
Input low voltage	V_{IL}	V_{DD} = 1.8 V to 3.6 V		– 0.5	—	$V_{DD} \times 0.2$	V
Output high voltage	V_{OH}	I_{OH} = – 2 mA		$V_{DD} - 0.5$	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2 mA		—	—	0.4	V
Pull up resistance for $\overline{\text{HOLD}}$	R_P	—		36	66	230	kΩ

*1 : Applicable pin : $\overline{\text{CS}}$, $\overline{\text{WP}}$, SCK, SI

*2 : Applicable pin : SO

*3 : Input voltage magnitude : VDD – 0.2 V or VSS

2. AC Characteristics

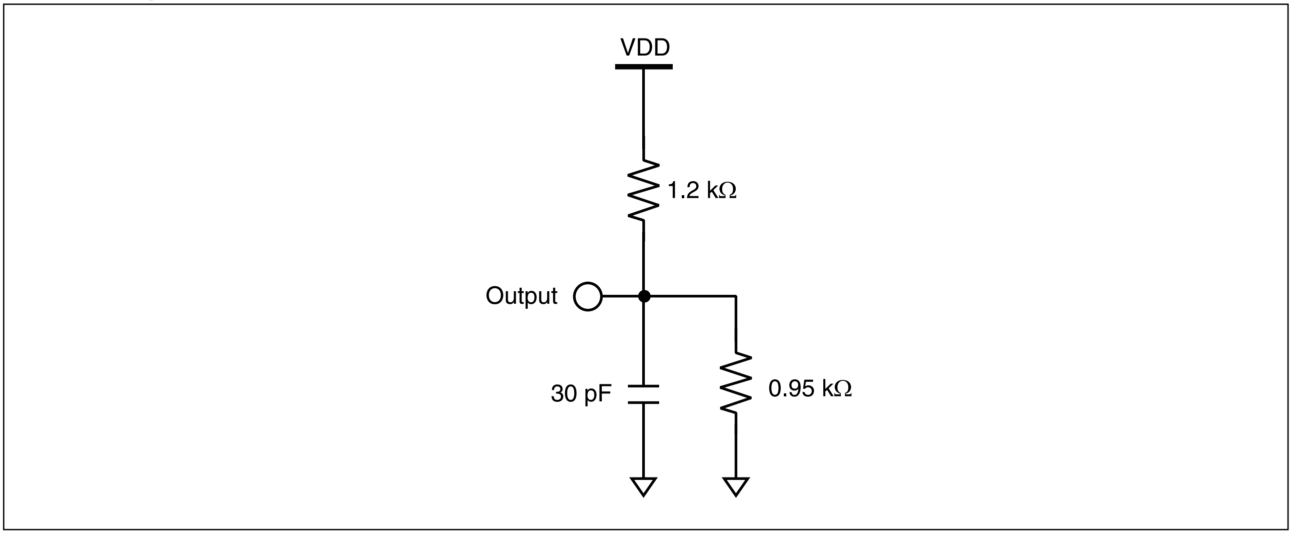
Parameter	Symbol	Value		Unit	Condition
		Min	Max		V_{DD}
SCK clock frequency	f_{CK}	—	50	MHz	all commands except for READ/ SSRD
		—	40		READ command
		—	10		SSRD command
Clock high time	t_{CH}	9	—	ns	
Clock low time	t_{CL}	9	—	ns	
Chip select set up time	t_{CSU}	5	—	ns	
Chip select hold time	t_{CSH}	5	—	ns	
Output disable time	t_{OD}	—	10	ns	
Output data valid time	t_{ODV}	—	8	ns	*1
Output hold time	t_{OH}	0	—	ns	
Deselect time	t_{D}	40	—	ns	
Data in rising time	t_{R}	—	50	ns	
Data falling time	t_{F}	—	50	ns	
Data set up time	t_{SU}	5	—	ns	
Data hold time	t_{H}	5	—	ns	
$\overline{\text{HOLD}}$ set uptime	t_{HS}	10	—	ns	—
$\overline{\text{HOLD}}$ hold time	t_{HH}	10	—	ns	—
$\overline{\text{HOLD}}$ output floating time	t_{HZ}	—	20	ns	—
$\overline{\text{HOLD}}$ output active time	t_{LZ}	—	20	ns	—
DPD/Hibernate recovery pulse width	t_{CSWL}	100	—	ns	
DPD recovery time	t_{RECDPD}	—	10	µs	
Hibernate recovery time	t_{RECHIB}	—	450	µs	

*1: In SSRD command, 60ns(max.)

AC Test Condition

Power supply voltage : 1.8 V to 3.6 V Operation
Operation ambient temperature : − 40 °C to + 125 °C
Input voltage magnitude : $V_{DD} \times 0.8 \leq V_{IH} \leq V_{DD}$
$0 \leq V_{IL} \leq V_{DD} \times 0.2$
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

AC Load Equivalent Circuit

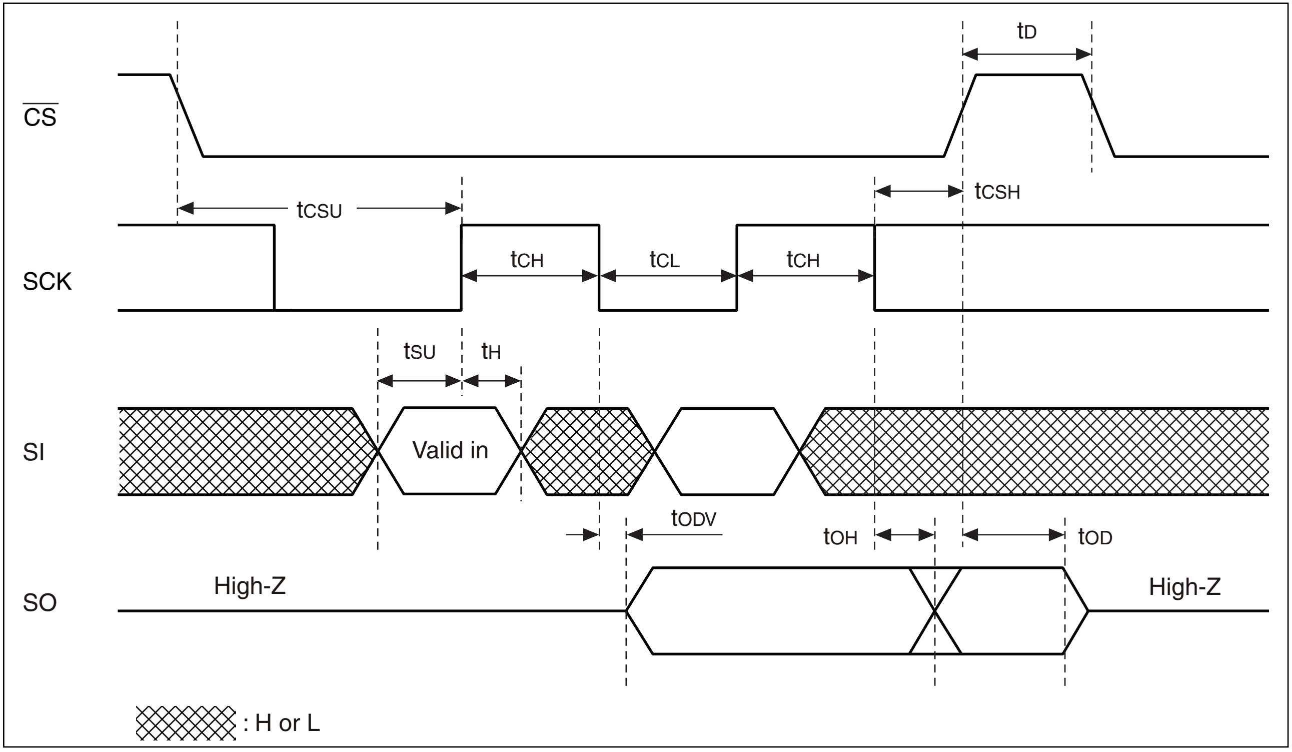

VDD
1.2 kΩ
Output
30 pF
0.95 kΩ

3. Pin Capacitance

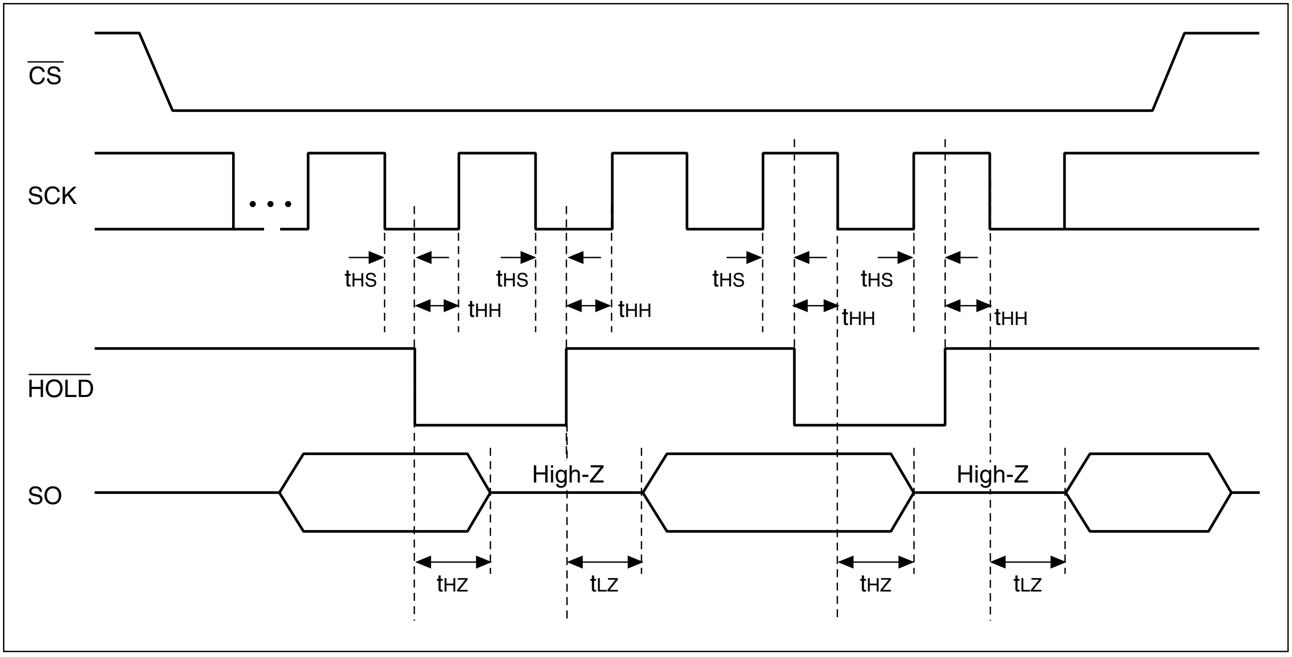
Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	C_O	V_{DD} = 3.3 V, V_{IN} = V_{OUT} = 0 V to V_{DD}, f = 1 MHz, T_A = +25 °C	—	8	pF
Input capacitance	C_I		—	6	pF

■ TIMING DIAGRAM

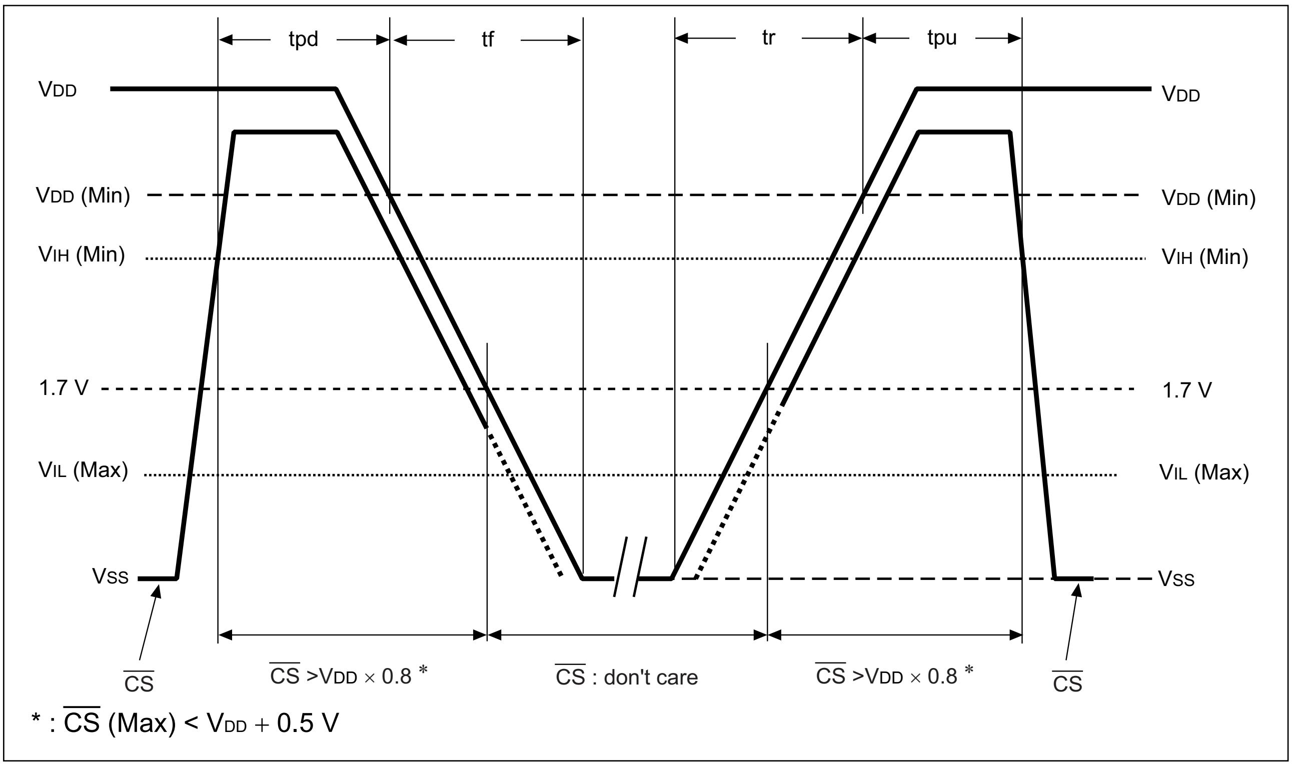
• Serial Data Timing


CS
SCK
SI
SO
tD
tCSU
tCSH
tCH
tCL
tCH
tSU
tH
Valid in
tODV
tOH
tOD
High-Z
High-Z
▨ : H or L

• Hold Timing


CS
SCK
HOLD
SO
tHS
tHH
tHS
tHH
tHS
tHH
tHS
tHH
High-Z
High-Z
tHZ
tLZ
tHZ
tLZ

■ POWER ON/OFF SEQUENCE


tpd
tf
tr
tpu
VDD
VDD
VDD (Min)
VDD (Min)
VIH (Min)
VIH (Min)
1.7 V
1.7 V
VIL (Max)
VIL (Max)
VSS
VSS
CS
CS >VDD × 0.8 *
CS : don't care
CS >VDD × 0.8 *
CS
* : CS (Max) < VDD + 0.5 V

In case relative short V_{DD} pulse whose peak level is beyond 1.7 is applied, please set V_{DD} falling time, tf, longer than 0.4ms/V. (When V_{DD} rises beyond 1.7V, and falls just after, if this term is very short the device may loose its function.)

Parameter	Symbol	Value		Unit	Condition
		Min	Max		V_{DD}
$\overline{\text{CS}}$ level hold time at power OFF	tpd	400	—	ns	1.8V to 2.7V
		0	—		2.7V to 3.6V
$\overline{\text{CS}}$ level hold time at power ON	tpu	450	—	µs	—
Power supply rising time	tr	0.05	—	ms/V	—
Power supply falling time	tf	0.1	—	ms/V	—

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance[*1]	10^{13}	—	Times	Operation Ambient Temperature $T_A = +125$ °C
Data Retention[*2]	5.9 or more[*3]	—	Years	Operation Ambient Temperature $T_A = +125$ °C
	19.1	—		Operation Ambient Temperature $T_A = +105$ °C
	70.4	—		Operation Ambient Temperature $T_A = +85$ °C

*1:The value for Read/Write endurance apply to the total number of read and write operations per row in FeRAM. This is because FeRAM needs writing operation after each reading operations. Each row in the memory array has 32 internal outputs, and 8 outputs are selected by A0 and A1. In continuous Read/Write operations, after selecting a certain address and automatically incrementing until A0 and A1 change from (0,0) to (1,1), the Read/Write count endurance count is totaled as one operation. Subsequently, when incrementing automatically and switching to the next row, each row is counted as a new Read/Write operation. If /CS is raised and then the same row is selected again, it is counted as the second operation for that row.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

*3: Under evaluation for more than 5.9 years(+125 °C).

■ NOTE ON USE

We recommend programming of the device after reflow except for special sector region and serial number region. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JEDEC JS001 compliant	MS85RS1MTYPNF-GS-BDE1 MS85RS1MTYPNF-GS-BDERE1 MS85RS1MTYPN-GS-AWE1 MS85RS1MTYPN-GS-AWEWE1	≥ |2000 V|
ESD CDM (Charged Device Model) JEDEC JS002 compliant		≥ |1000 V|
Latch-Up (I-test) JESD78 compliant		≥ |125mA|
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		≥ 5.4V

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ Current status on Contained Restricted Substances

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

■ ORDERING INFORMATION :

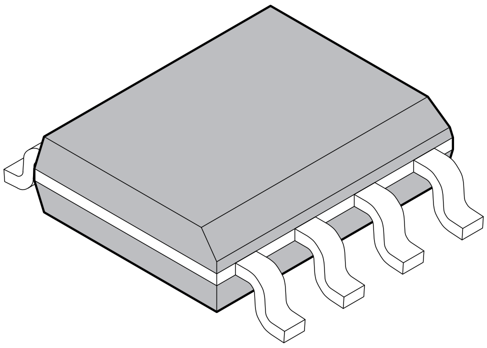
Part number	Package	Shipping form	Minimum shipping quantity
MS85RS1MTYPNF-GS-BDE1	8-pin plastic SOP	Tube	— *
MS85RS1MTYPNF-GS-BDERE1	8-pin plastic SOP	Embossed Carrier tape	1500
MS85RS1MTYPN-GS-AWE1	8-pin plastic DFN	Tray	— *
MS85RS1MTYPN-GS-AWEWE1	8-pin plastic DFN	Embossed Carrier tape	1500

* : Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSION

(1) MS85RS1MTYPNF-GS-BDE1/MS85RS1MTYPNF-GS-BDERE1

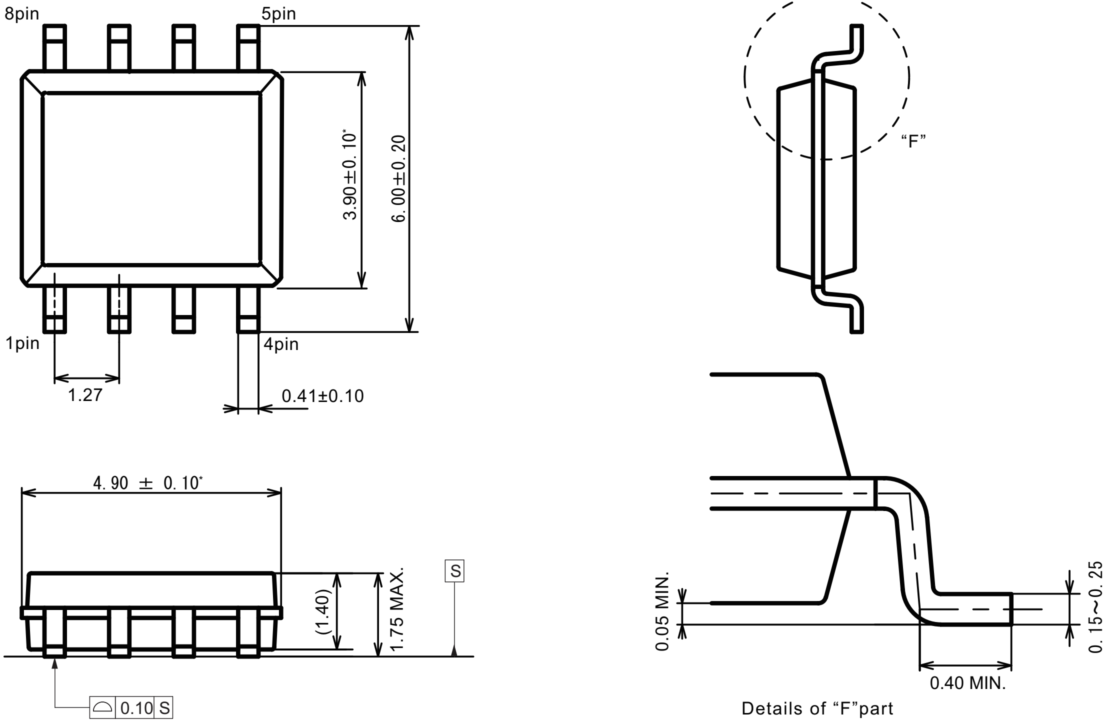
8-pin plastic SOP(150mil)



Lead pitch	1.27㎜
Package width x Package length	3.90mm x 4.90mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.75mm MAX.

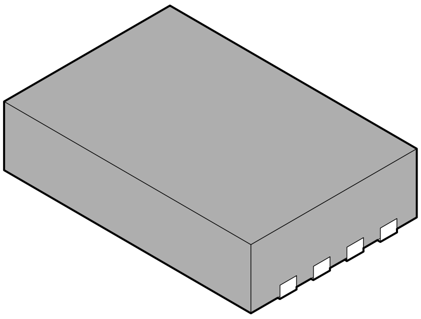
8-pin plastic SOP

Note *: These dimension do not include resin protrution.
Pins width do not include tie bar cutting remaindar.

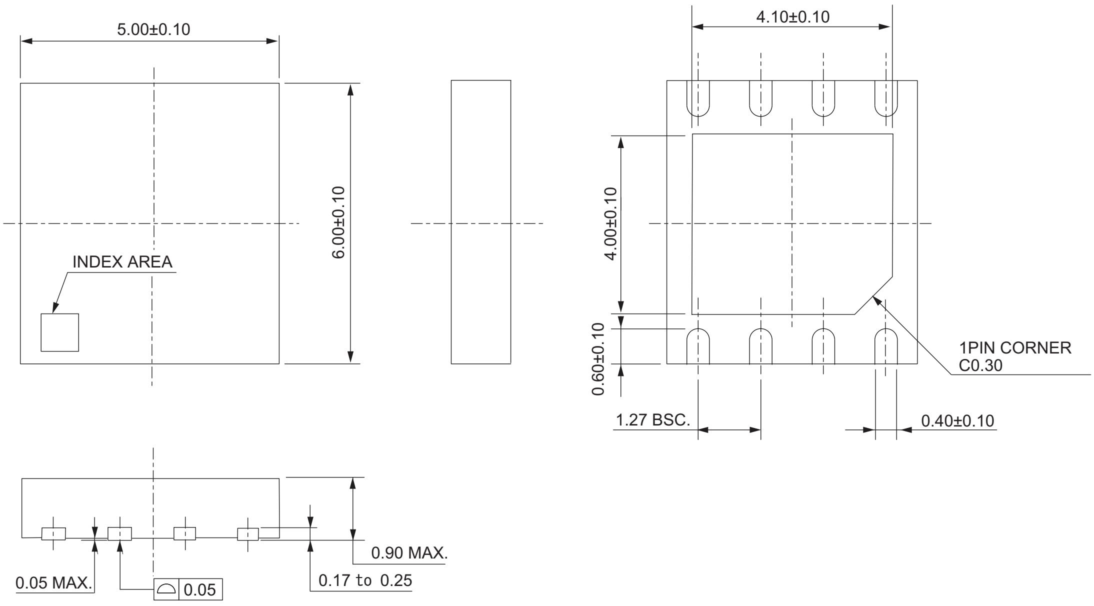

8pin
5pin
1pin
4pin
3.90±0.10*
6.00±0.20
1.27
0.41±0.10
4.90 ± 0.10*
(1.40)
1.75 MAX.
S
0.10 S
"F"
0.05 MIN.
0.15~0.25
0.40 MIN.
Details of "F"part

Dimension in mm

(2) MS85RS1MTYPN-GS-AWE1/MS85RS1MTYPN-GS-AWEWE1

8-pin plastic DFN 	Lead pitch	1.27 mm
	Package width x Package length	5.00 mm × 6.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX

8-pin plastic DFN

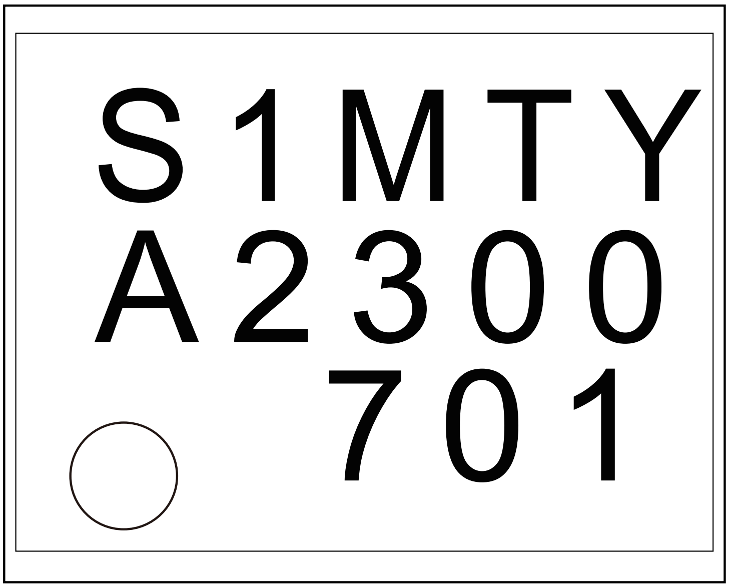

5.00±0.10
6.00±0.10
INDEX AREA
4.10±0.10
4.00±0.10
0.60±0.10
1PIN CORNER
C0.30
1.27 BSC.
0.40±0.10
0.90 MAX.
0.05 MAX.
0.05
0.17 to 0.25

Dimensions in mm.

■ MARKING (Example)

(1) MS85RS1MTYPNF-GS-BDE1/MS85RS1MTYPNF-GS-BDERE1

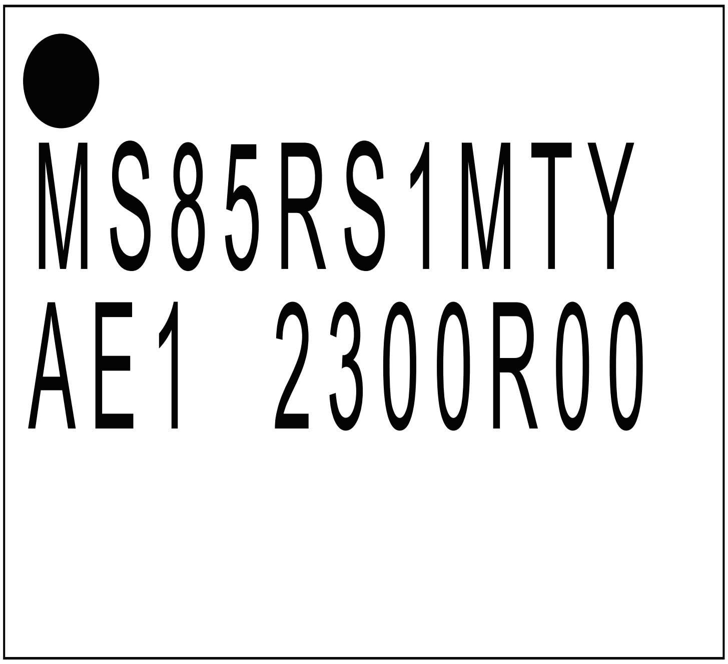
[MS85RS1MTYPNF-GS-BDE1]
[MS85RS1MTYPNF-GS-BDERE1]



S1MTY: Product name
A2300 : A(CS code) + 2300(Year and Week code)
701 : Trace code

(2) MS85RS1MTYPN-GS-AWE1/MS85RS1MTYPN-GS-AWEWE1

[MS85RS1MTYPN-GS-AWE1]
[MS85RS1MTYPN-GS-AWEWE1]



MS85RS1MTY: Product name
AE1 : A(CS code) + E1(Lead free code)
2300R00 : 2300(Year and Week code) + R00(Trace code)

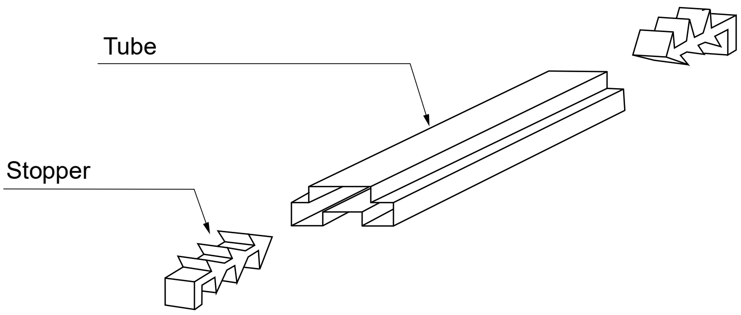
■ PACKING INFORMATION

(1) MS85RS1MTYPNF-GS-BDE1/MS85RS1MTYPNF-GS-BDERE1

1. **Tube** (MS85RS1MTYPNF-GS-BDE1)

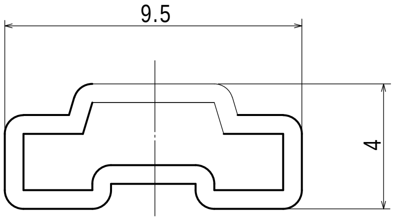
1.1 Tube Dimensions

- Tube/stopper shape (example)



- **Tube cross-sections** and Maximum quantity

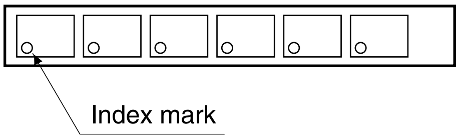
Maximum quantity		
pcs/tube(500mm)	pcs/inner box	pcs/outer box
85	4,250	17,000



No heat resistance.
Package should not be baked by using tube.

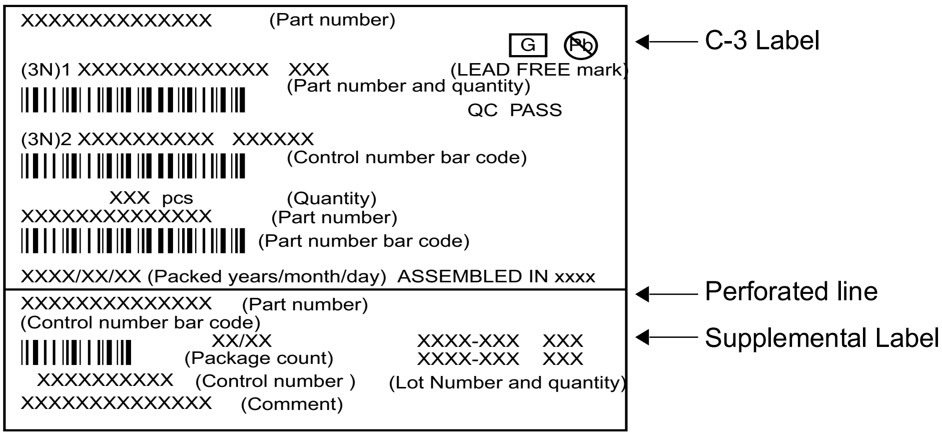
(Dimensions in mm)

- **Direction of index in tube**



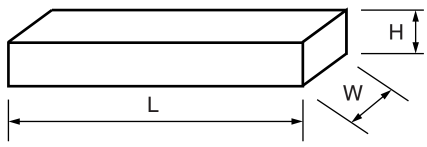
1.2 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Part number)
G
Pb
(3N)1 XXXXXXXXXXXXXX XXX
(LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)
XXX pcs
(Quantity)
XXXXXXXXXXXXXX
(Part number)
(Part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number)
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)
C-3 Label
Perforated line
Supplemental Label

1.3 Dimensions for Containers

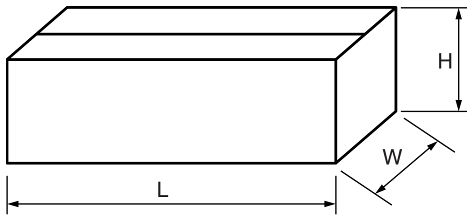
(1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



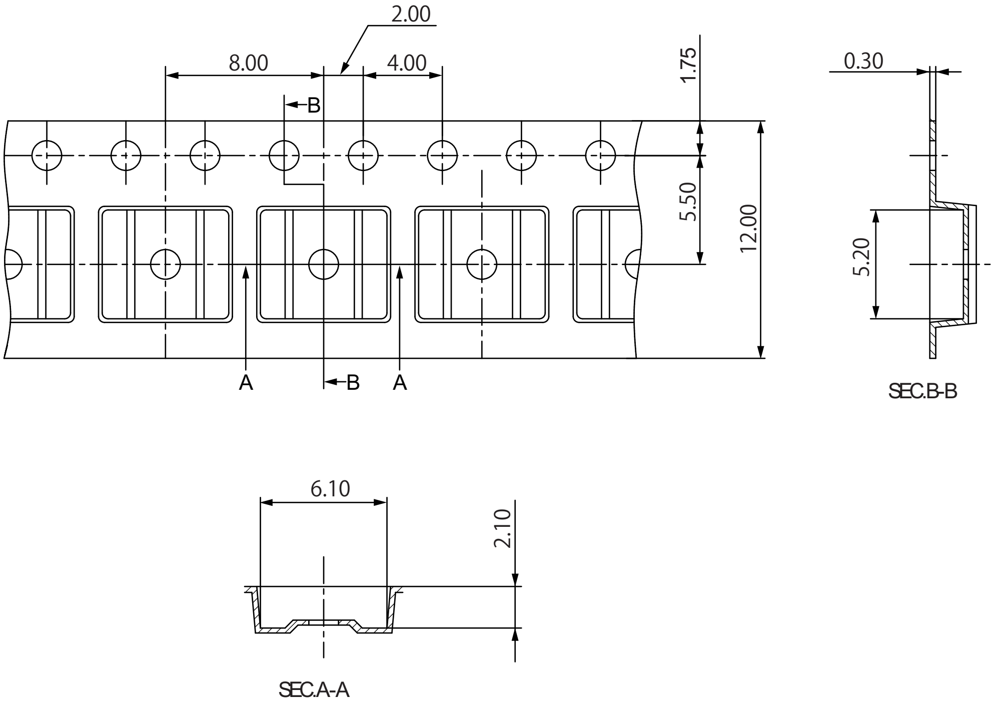
L	W	H
565	270	180

(Dimensions in mm)

2. Emboss Tape (MS85RS1MTYPNF-GS-BDERE1)

2.1 Tape Dimensions (not drawn to scale) (8-pin plastic SOP)

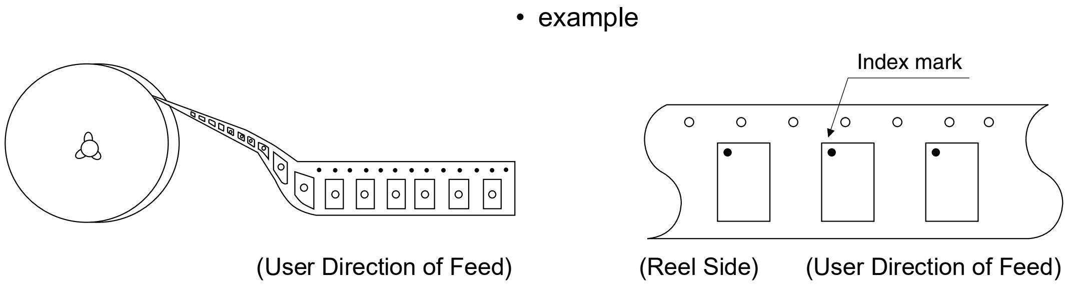
Maximum storage capacity		
pcs/reel(Φ254mm)	pcs/inner box	pcs/outer box
1500	1500 (1 pack/inner box)	9000 (6 inner boxes/outer box:Max)


2.00
8.00
4.00
B
1.75
5.50
12.00
A
B
A
0.30
5.20
SEC.B-B
6.10
2.10
SEC.A-A

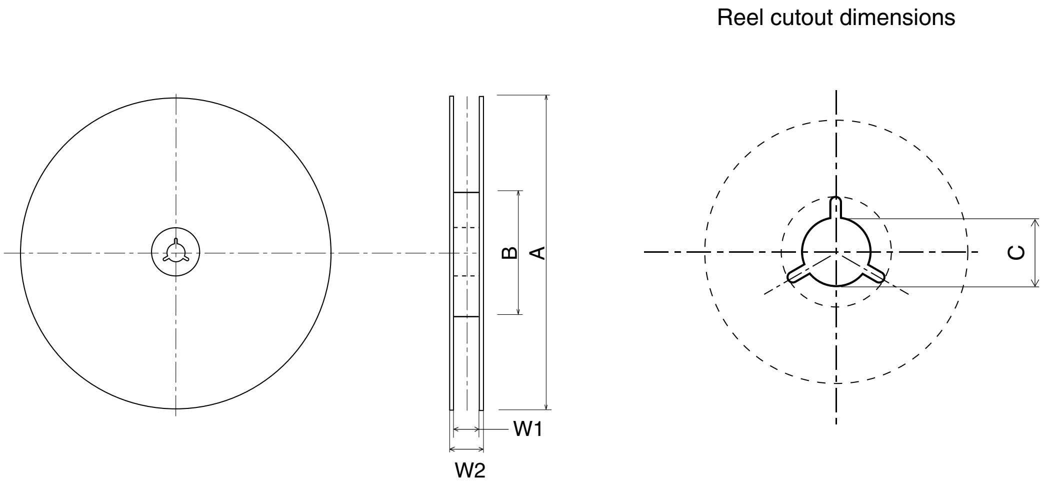
(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked by
using tape and reel.

2.2 IC orientation


• example
Index mark
(User Direction of Feed)
(Reel Side)
(User Direction of Feed)

2.3 Reel dimensions

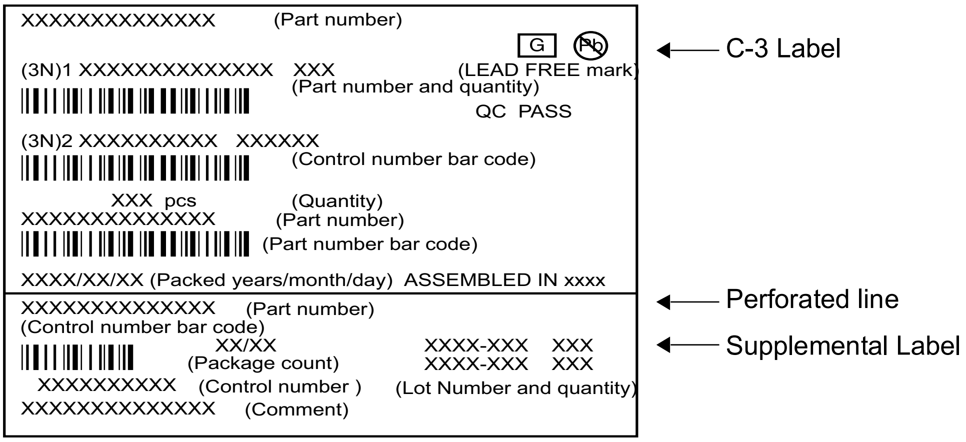

Reel cutout dimensions
B
A
C
W1
W2

Dimensions in mm

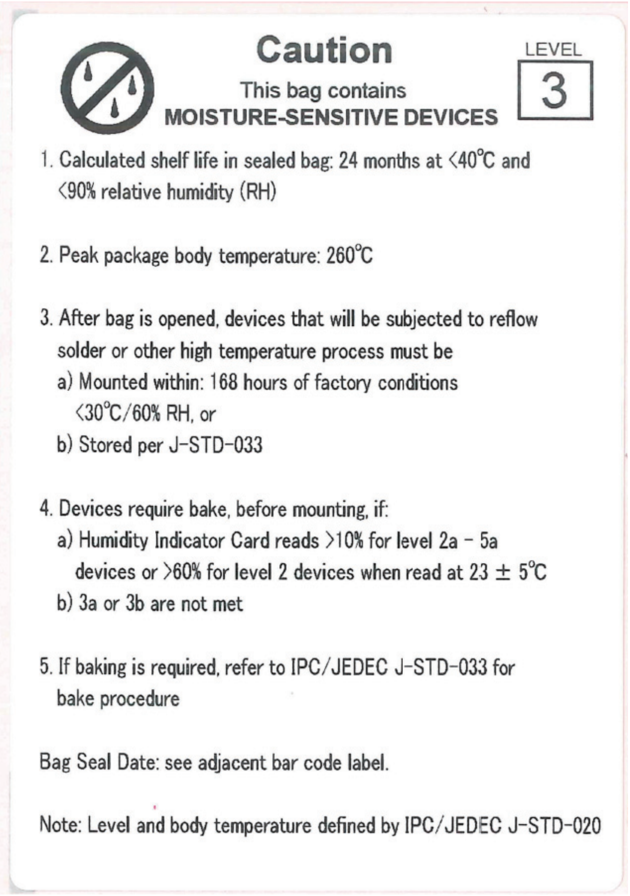
A	B	C	W1	W2
254	100	13	13.5	17.5

2.4 Product label indicators (examples)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Part number)
G
Pb
(3N)1 XXXXXXXXXXXXXX XXX (LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)
XXX pcs (Quantity)
XXXXXXXXXXXXXX (Part number)
(Part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number)
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)
C-3 Label
Perforated line
Supplemental Label

Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)
[MSL Label]



Caution

This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
3

1. Calculated shelf life in sealed bag: 24 months at <40°C and <90% relative humidity (RH)

2. Peak package body temperature: 260°C

3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   - a) Mounted within: 168 hours of factory conditions <30°C/60% RH, or
   - b) Stored per J-STD-033

4. Devices require bake, before mounting, if:
   - a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C
   - b) 3a or 3b are not met

5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure

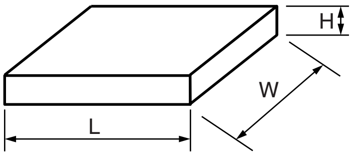
Bag Seal Date: see adjacent bar code label.

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

MSL label

2.5 Dimensions for Containers

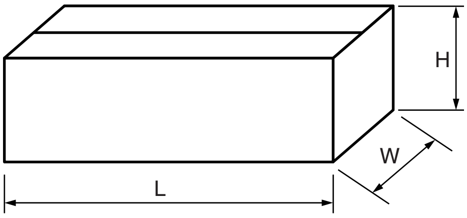
(1) Dimensions for inner box



Tape width	L	W	H
12	265	260	50

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
565	270	180

(Dimensions in mm)

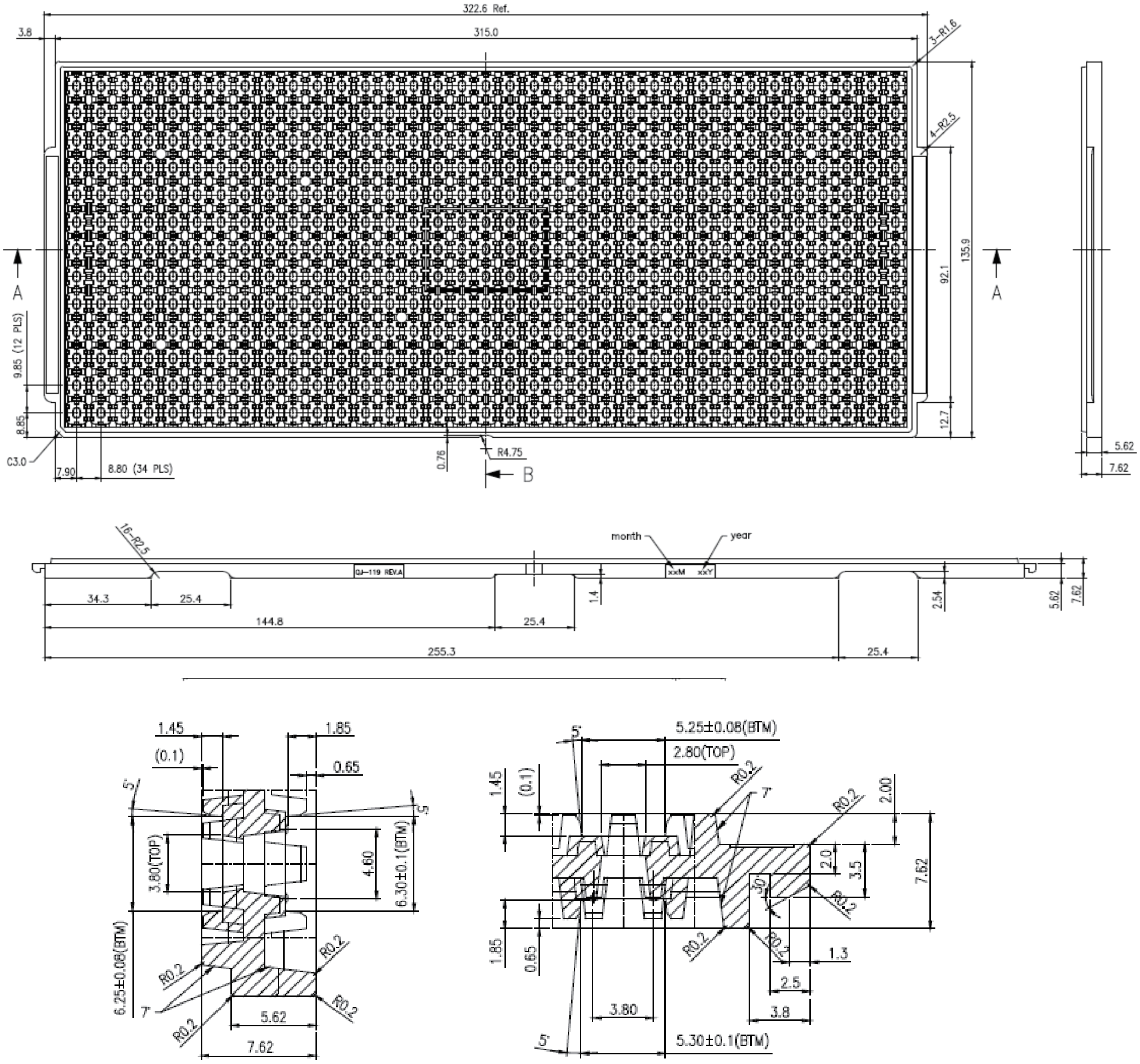
(2) MS85RS1MTYPN-GS-AWE1/MS85RS1MTYPN-GS-AWEWE1

1. **Tray** (MS85RS1MTYPN-GS-AWE1)

1.1 Tray Dimensions

DFN8

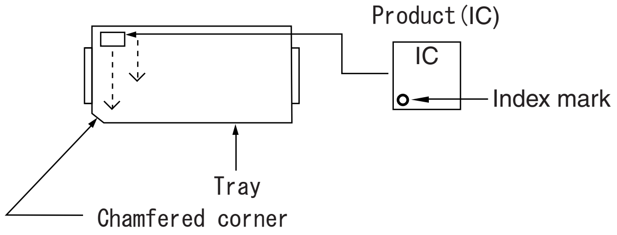
Maximum storage capacity		
pcs/tray	pcs/inner box	pcs/outer box
455	4550	9100


322.6 Ref.
315.0
3.8
3-R1.6
4-R2.5
135.9
92.1
12.7
A
A
9.85 (12 PLS)
8.85
C3.0
7.90
8.80 (34 PLS)
0.76
R4.75
B
5.62
7.62
16-R2.5
month
year
GJ-119 REV.A
xxM
xxY
34.3
25.4
144.8
25.4
255.3
25.4
1.4
2.54
5.62
7.62
1.45
(0.1)
1.85
0.65
5°
5°
3.80(TOP)
4.60
6.30±0.1(BTM)
6.25±0.08(BTM)
R0.2
R0.2
R0.2
R0.2
7°
5.62
7.62
5°
5.25±0.08(BTM)
2.80(TOP)
R0.2
7°
R0.2
2.00
1.45
(0.1)
2.0
3.5
7.62
30°
R0.2
R0.2
R0.2
1.3
2.5
3.8
1.85
0.65
3.80
5°
5.30±0.1(BTM)

(Dimensions in mm)

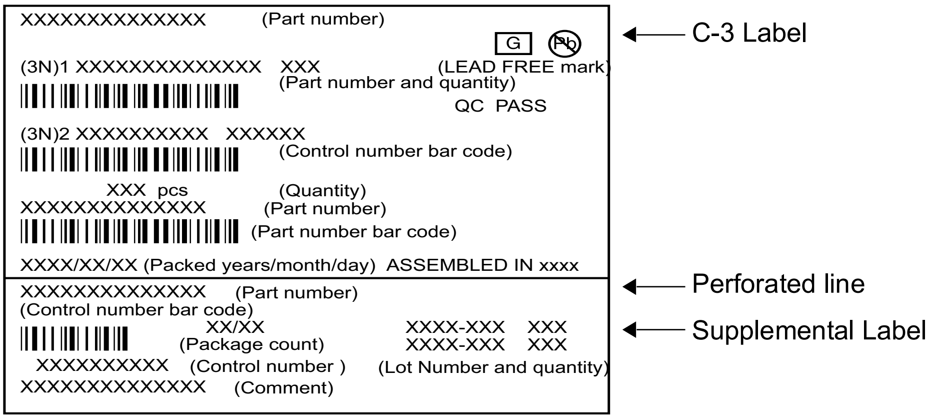
Heat proof temperature : 150 °C Max

1.2 IC orientation


Product (IC)
IC
Index mark
Tray
Chamfered corner

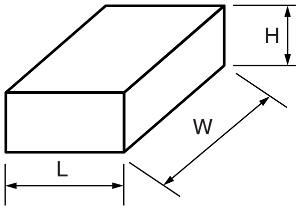
1.3 Product label indicators(example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Part number)
G
Pb
(3N)1 XXXXXXXXXXXXXX XXX
(LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)
XXX pcs
(Quantity)
XXXXXXXXXXXXXX
(Part number)
(Part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number)
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)
C-3 Label
Perforated line
Supplemental Label

1.4 Dimensions for Containers

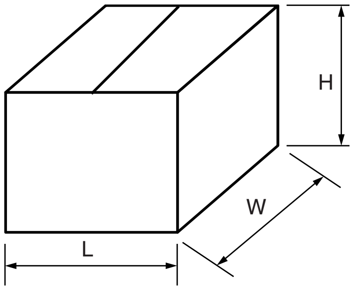
(1) Dimensions for inner box



L	W	H
175	375	110

(Dimensions in mm)

(2) Dimensions for outer box



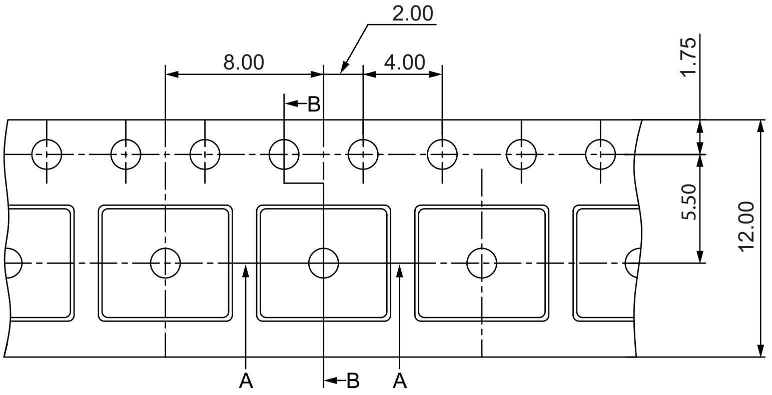
L	W	H
190	380	330

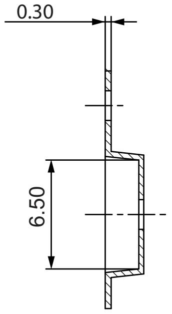
(Dimensions in mm)

2. **Emboss Tape** (MS85RS1MTYPN-GS-AWEWE1)

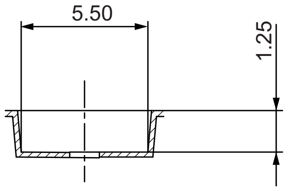
2.1 **Tape Dimensions** (not drawn to scale)(8-pin plastic DFN 5mm x 6mm)

Maximum storage capacity		
pcs/reel(Φ330mm)	pcs/inner box	pcs/outer box
1500	1500 (1 pack/inner box)	7500 (5 inner boxes/outer box:Max)





SEC.B-B

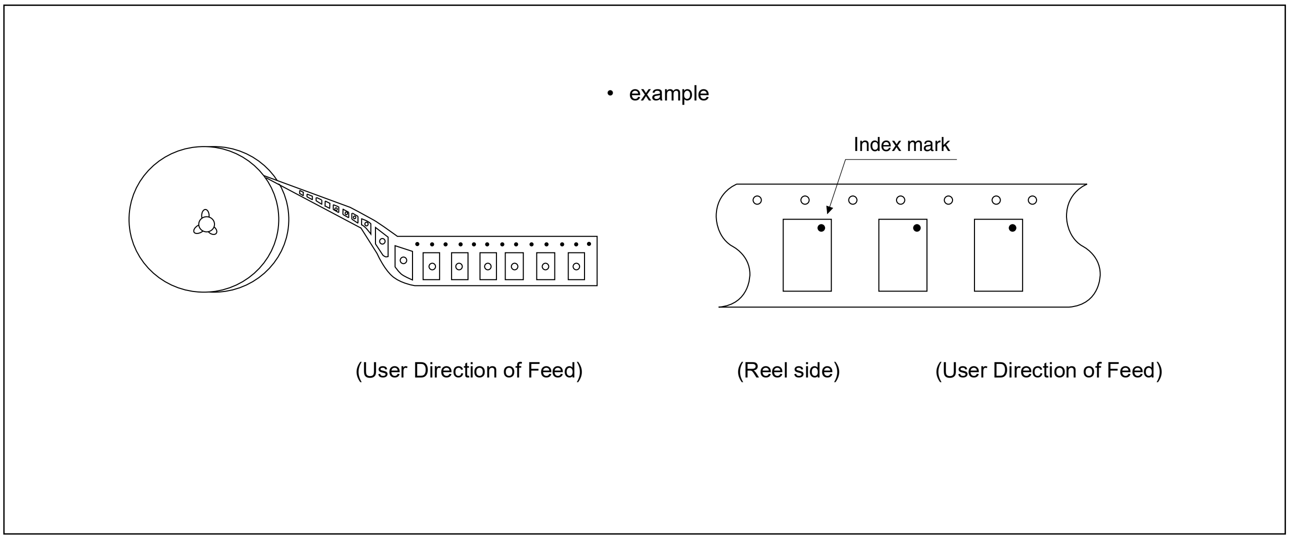


SEC.A-A

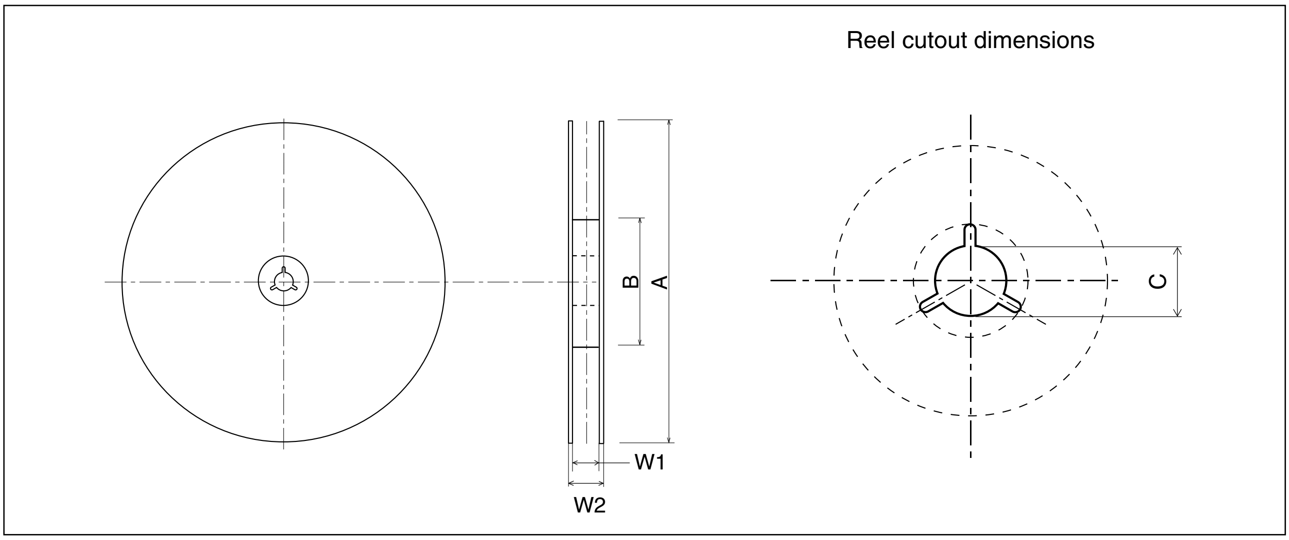
(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

2.2 IC orientation


• example
Index mark
(User Direction of Feed)
(Reel side)
(User Direction of Feed)

2.3 Reel dimensions

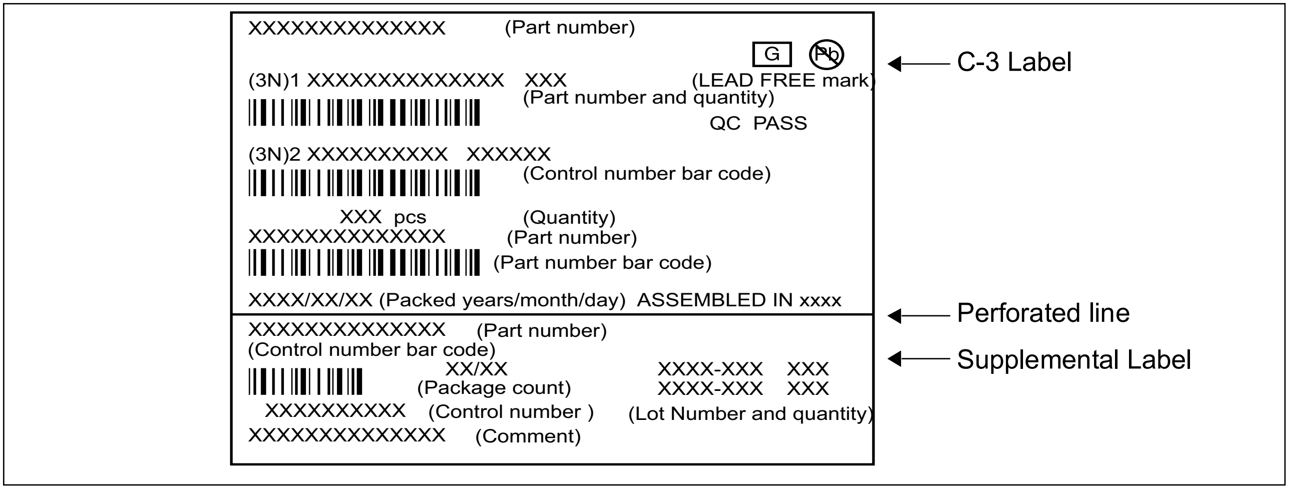

Reel cutout dimensions
B
A
C
W1
W2

Dimensions in mm

A	B	C	W1	W2
330	100	13	13.5	17.5

2.4 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



XXXXXXXXXXXXXX (Part number)

G Pb

(3N)1 XXXXXXXXXXXXXX XXX (LEAD FREE mark)
(Part number and quantity)

QC PASS

(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)

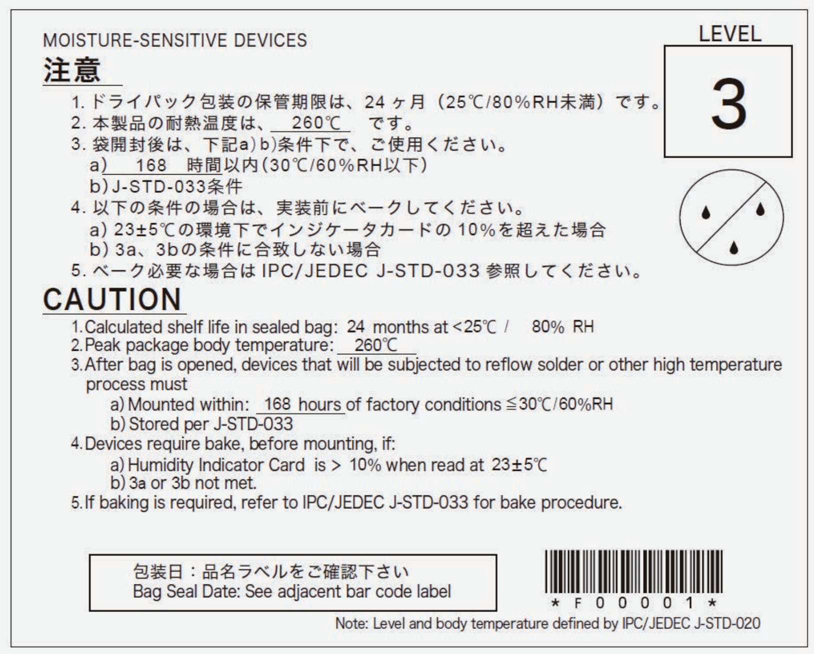
XXX pcs (Quantity)
XXXXXXXXXXXXXX (Part number)
(Part number bar code)

XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx

XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number)
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)

Label II:Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)

[MSL Label]



MOISTURE-SENSITIVE DEVICES

LEVEL 3

注意

1. ドライパック包装の保管期限は、24ヶ月（25℃/80%RH未満）です。
2. 本製品の耐熱温度は、260℃ です。
3. 袋開封後は、下記a)b)条件下で、ご使用ください。
   a) 168 時間以内(30℃/60%RH以下)
   b) J-STD-033条件
4. 以下の条件の場合は、実装前にベークしてください。
   a) 23±5℃の環境下でインジケータカードの 10%を超えた場合
   b) 3a、3bの条件に合致しない場合
5. ベーク必要な場合は IPC/JEDEC J-STD-033 参照してください。

CAUTION

1. Calculated shelf life in sealed bag: 24 months at <25℃ / 80% RH
2. Peak package body temperature: 260℃
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: 168 hours of factory conditions ≦30℃/60%RH
   b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is > 10% when read at 23±5℃
   b) 3a or 3b not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

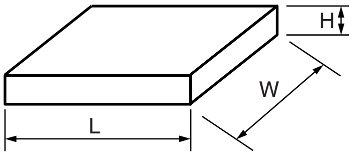
包装日：品名ラベルをご確認下さい
Bag Seal Date: See adjacent bar code label

* F 0 0 0 0 1 *

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

2.5 Dimensions for Containers

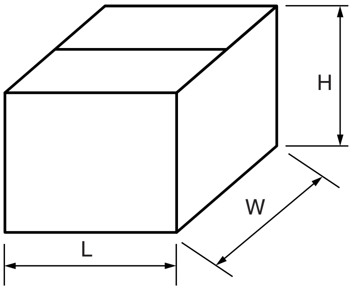
(1) Dimensions for inner box



Tape width	L	W	H
12	350	335	35

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
384	368	225

(Dimensions in mm)

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Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan
https://ramxeed.com/

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