

Memory FeRAM

64 K (8 K × 8) Bit SPI

MB85RS64T

■ DESCRIPTION

MB85RS64T is a FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 8,192 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

MB85RS64T adopts the Serial Peripheral Interface (SPI).

The MB85RS64T is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85RS64T can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E²PROM.

MB85RS64T does not take long time to write data like Flash memories or E²PROM, and MB85RS64T takes no wait time.

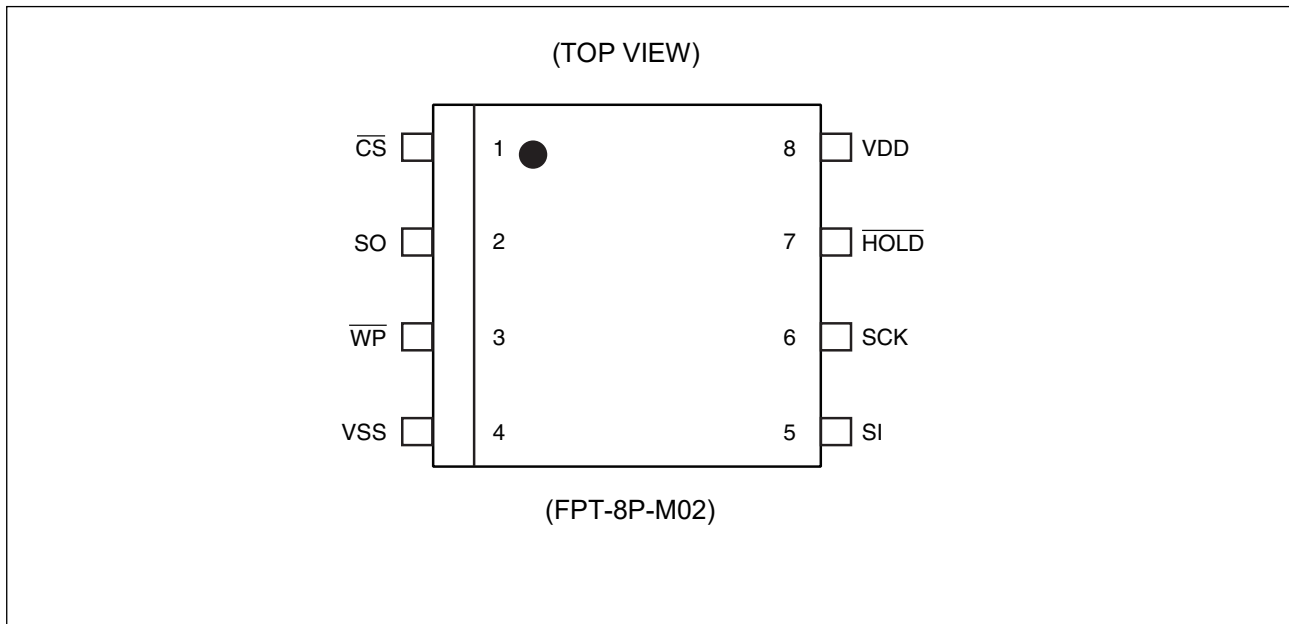
■ FEATURES

- Bit configuration : 8,192 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 10 MHz (Max)
- High endurance : 10^{13} times / byte
- Data retention : 40.2 years (+ 85 °C), 383 years (+ 55 °C)
- Operating power supply voltage : 1.7 V to 3.6 V
- Low power consumption : Operating power supply current 0.8 mA (Max@10 MHz)
Standby current 9 μA (Typ)
- Operation ambient temperature range : - 40 °C to +85 °C
- Package : 8-pin plastic SOP (FPT-8P-M02)
RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

MB85RS64T

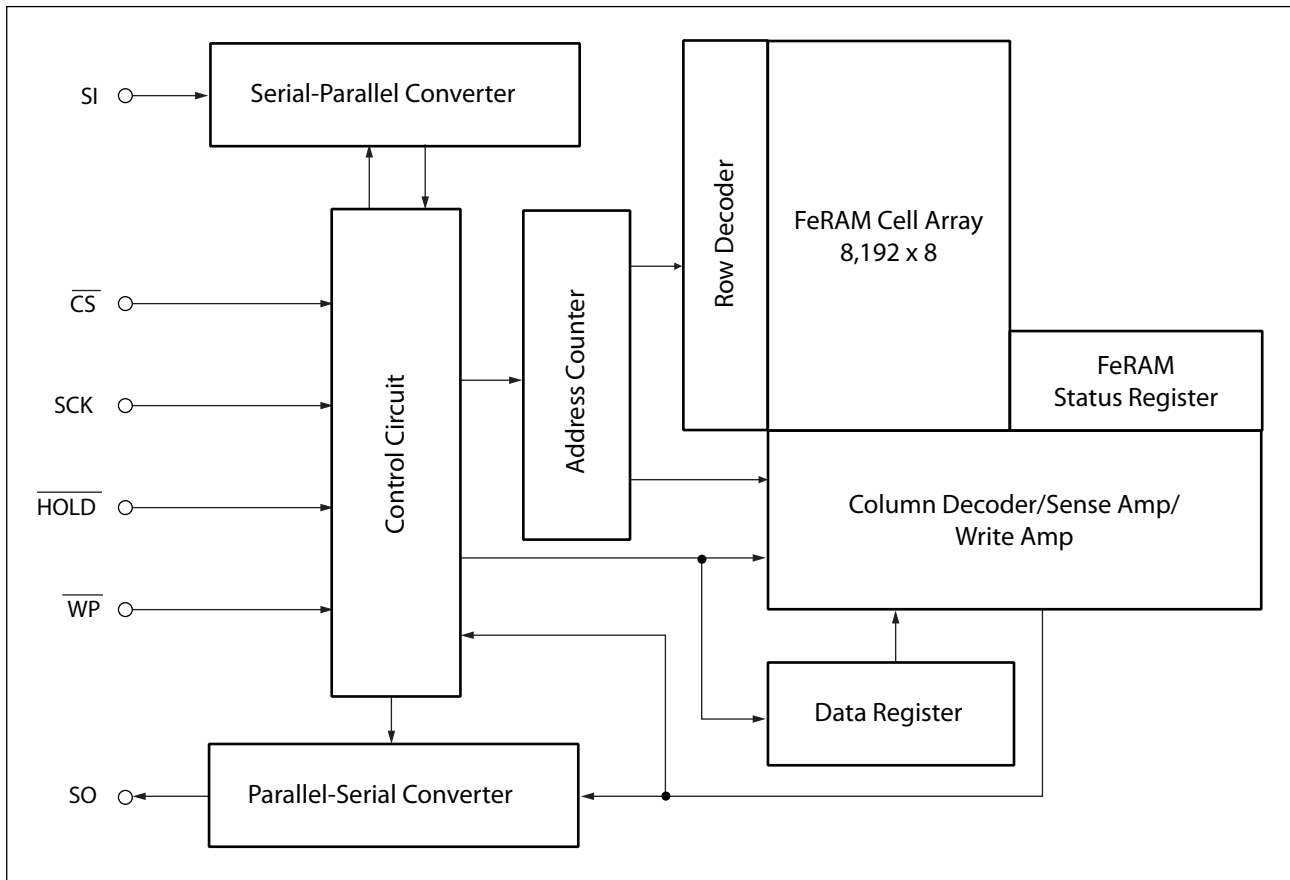
■ PIN ASSIGNMENT



■ PIN FUNCTIONAL DESCRIPTIONS

Pin No.	Pin Name	Functional description
1	\overline{CS}	Chip Select pin This is an input pin to make chip select. When \overline{CS} is the "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored at this time. When \overline{CS} is the "L" level, device is in select (active) status. \overline{CS} has to be the "L" level before inputting op-code.
3	\overline{WP}	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with \overline{WP} and WPEN. See "■ WRITING PROTECT" for detail.
7	\overline{HOLD}	Hold pin This pin is used to interrupt serial input/output without making chip deselect. When \overline{HOLD} is the "L" level, hold operation is activated, SO becomes High-Z, and SCK and SI become don't care. See "■ HOLD OPERATION" for detail.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FeRAM memory cell array and status register are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin
DIE PAD	—	It is allowed for the DIE PAD on the bottom of the SON8 package to be floating (no connection to anything) or to be connected to VSS.

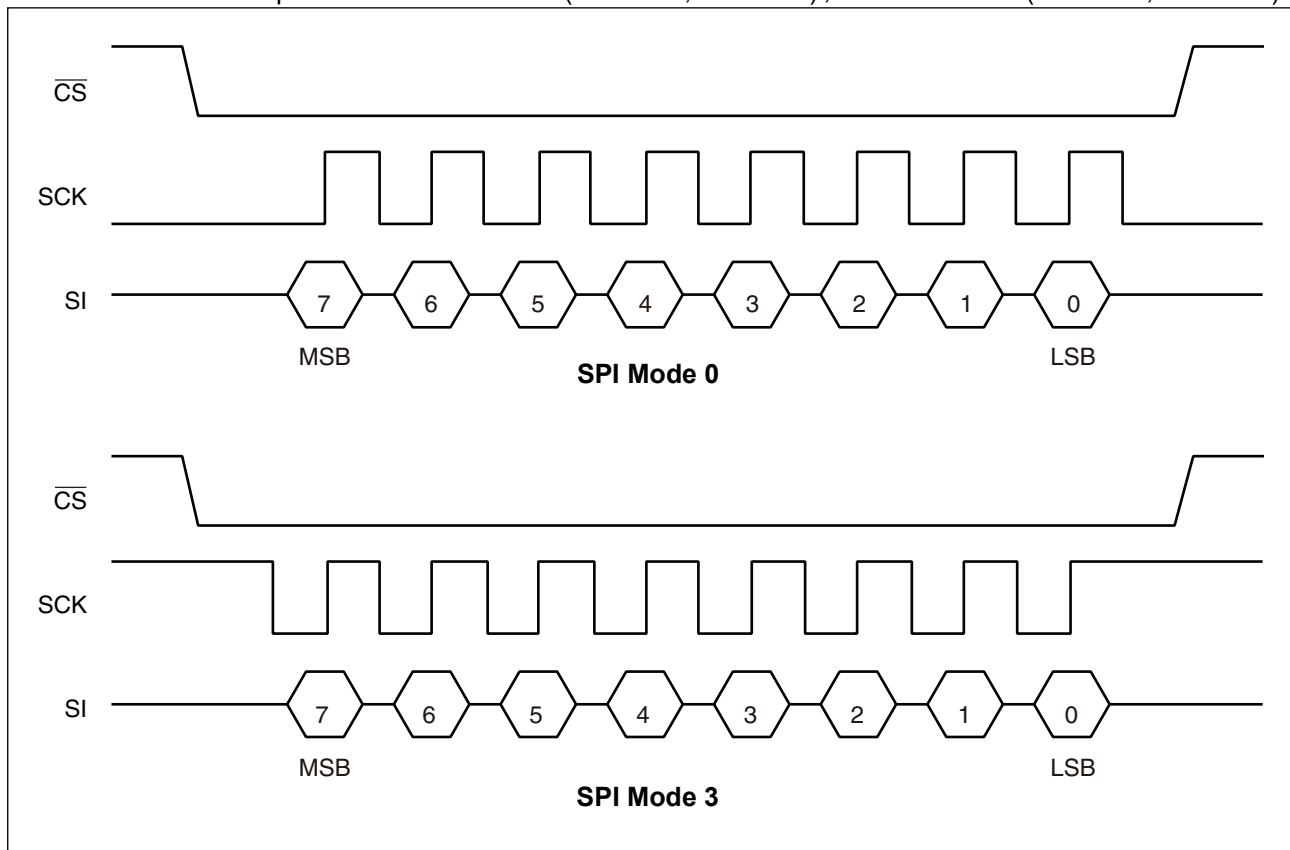
■ BLOCK DIAGRAM



MB85RS64T

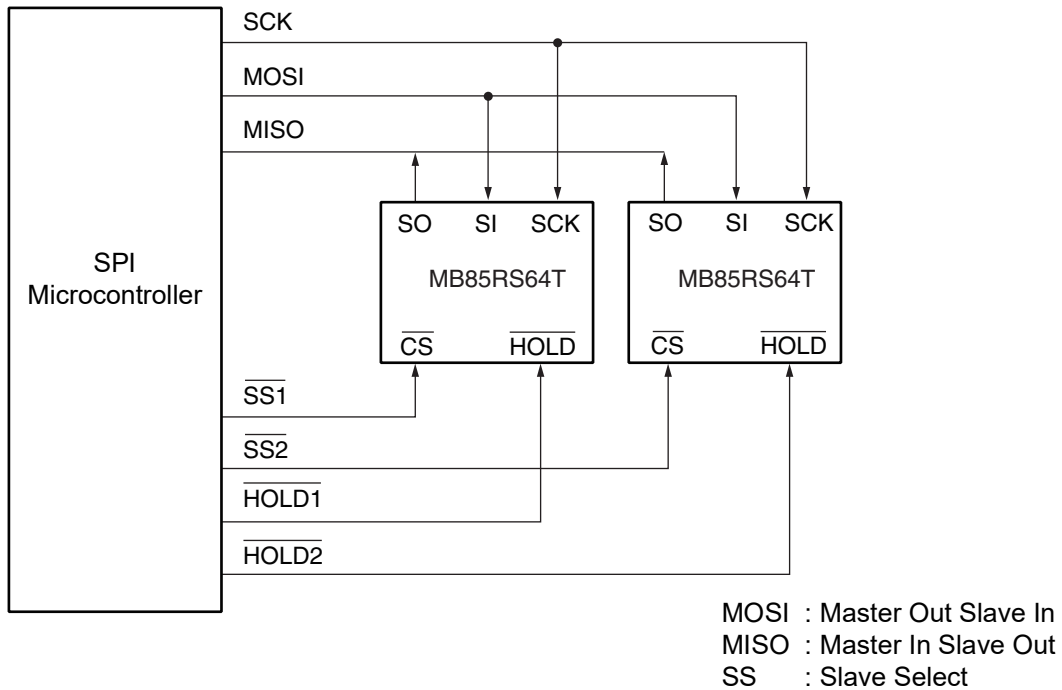
■ SPI MODE

MB85RS64T corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0), and SPI mode 3 (CPOL = 1, CPHA = 1).

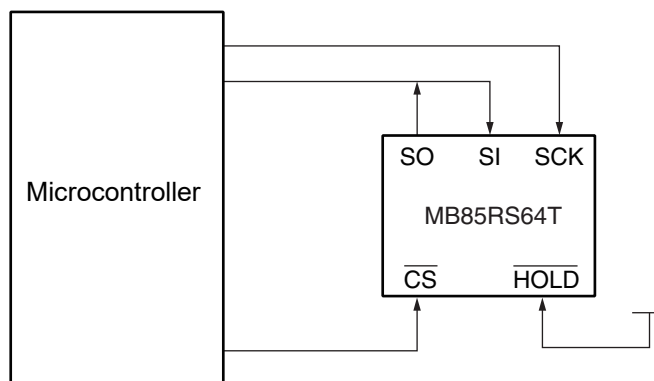


■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS64T works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



System Configuration with SPI Port



System Configuration without SPI Port

■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FeRAM). WPEN protects writing to a status register (see “■ WRITING PROTECT”) relating with \overline{WP} input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible, and “000” is written before shipment. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (see “■ BLOCK PROTECT”). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FeRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition.
0	0	This is a bit fixed to “0”.

■ OP-CODE

MB85RS64T accepts 8 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If CS is risen while inputting op-code, the command are not performed.

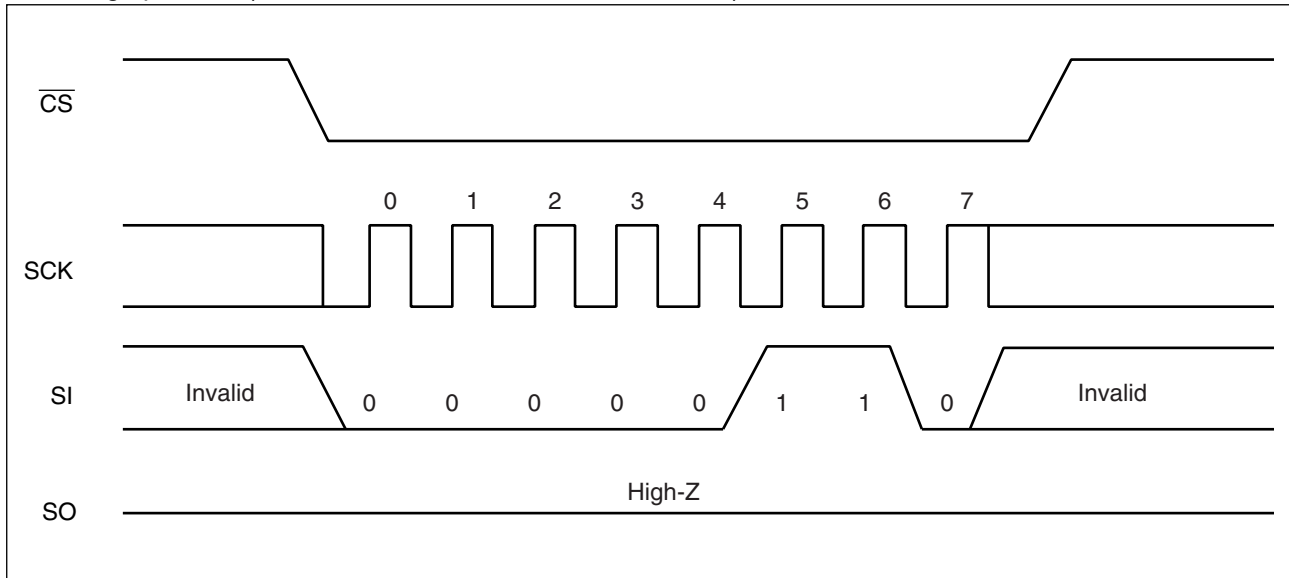
Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110 _B
WRDI	Reset Write Enable Latch	0000 0100 _B
RDSR	Read Status Register	0000 0101 _B
WRSR	Write Status Register	0000 0001 _B
READ	Read Memory Code	0000 0011 _B
WRITE	Write Memory Code	0000 0010 _B
RDID	Read Device ID	1001 1111 _B
SLEEP	Sleep Mode	1011 1001 _B
RFU	Reserved for future use ^{*1}	0000 1011 _B

*1:When this command is input, SO output will be unvalued.

■ COMMAND

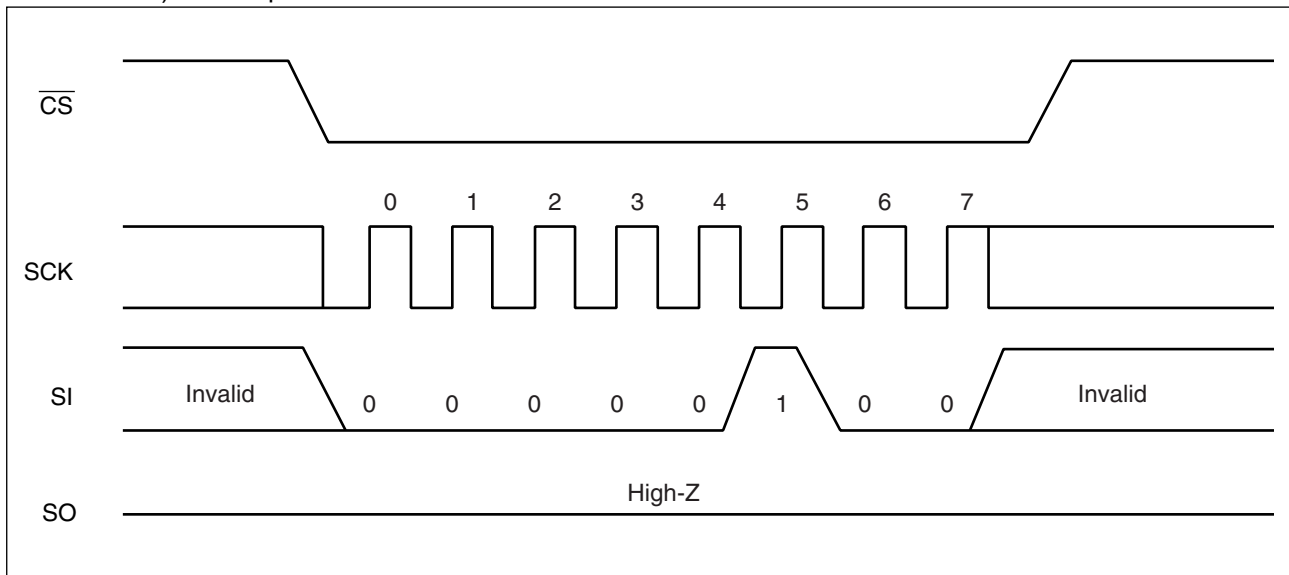
• WREN

The WREN command sets WEL (Write Enable Latch) . WEL shall be set with the WREN command before writing operation (WRSR command and WRITE command) .



• WRDI

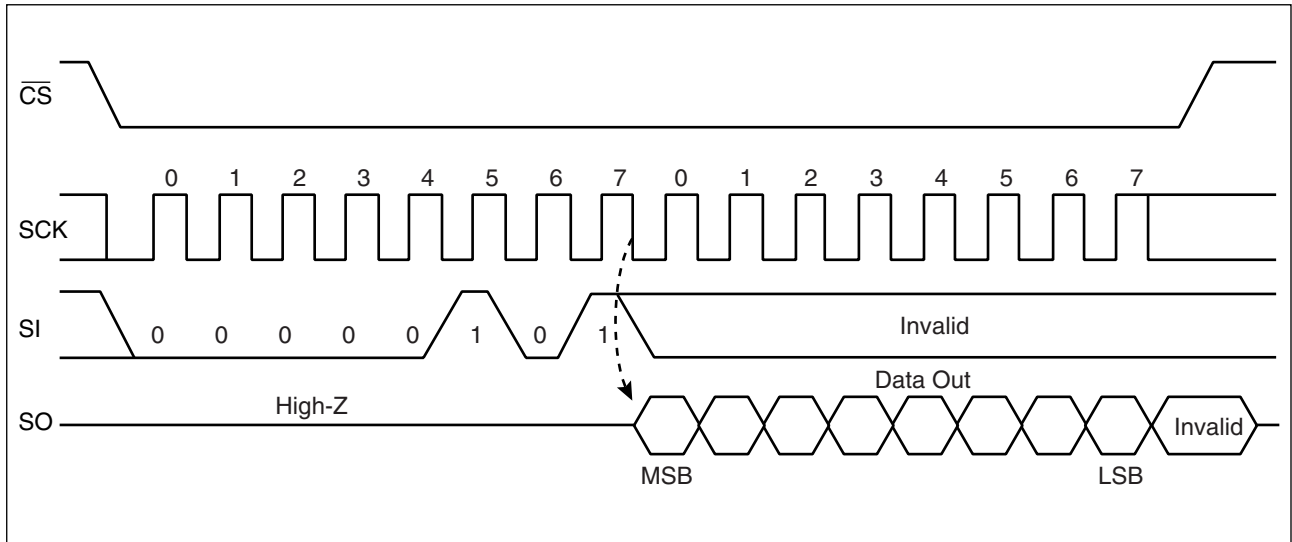
The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRITE command and WRSR command) are not performed when WEL is reset.



MB85RS64T

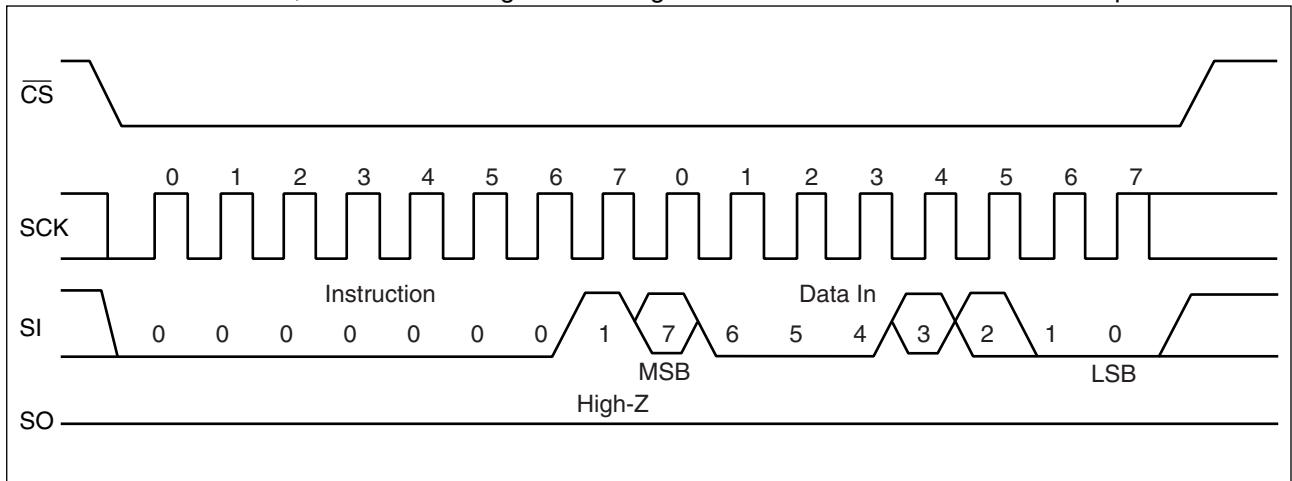
• RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid during this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of \overline{CS} .



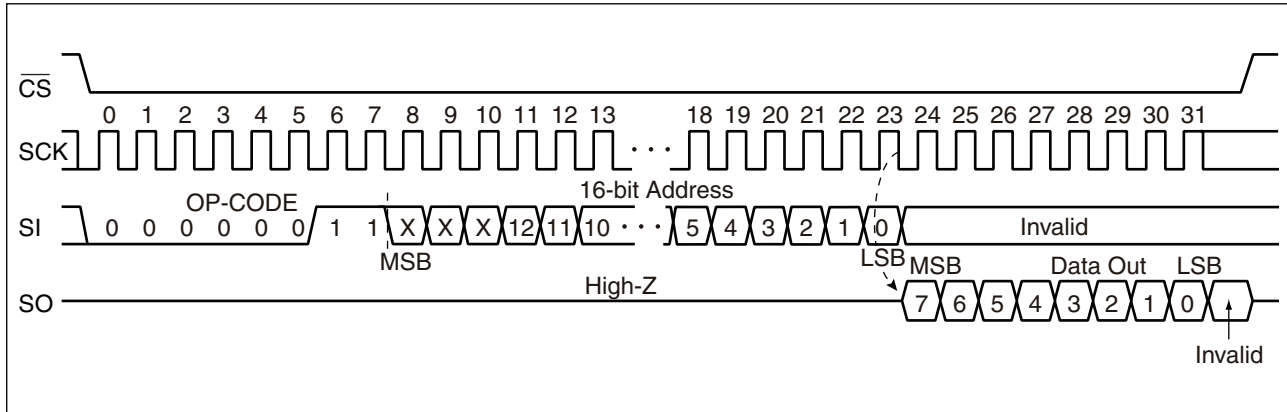
• WRSR

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored. The \overline{WP} signal level shall be fixed before performing the WRSR command, and do not change the \overline{WP} signal level until the end of command sequence.



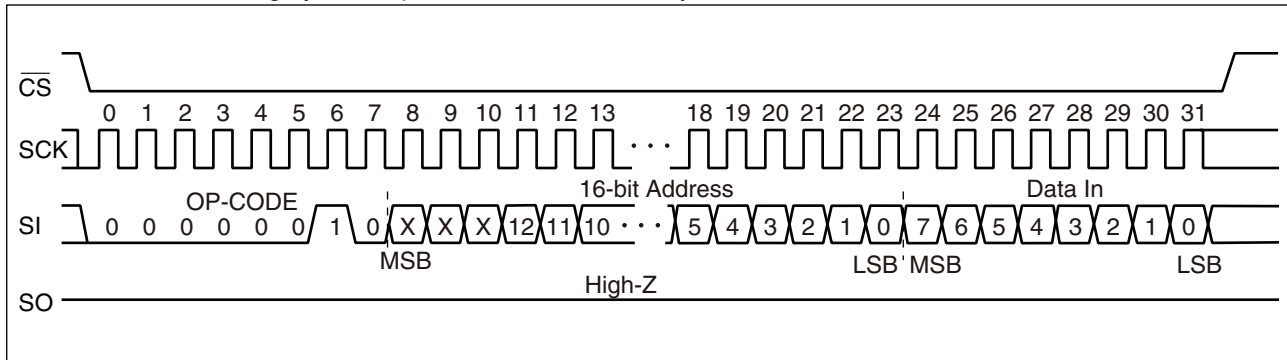
• READ

The READ command reads FeRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The 3-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When \overline{CS} is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before \overline{CS} rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.



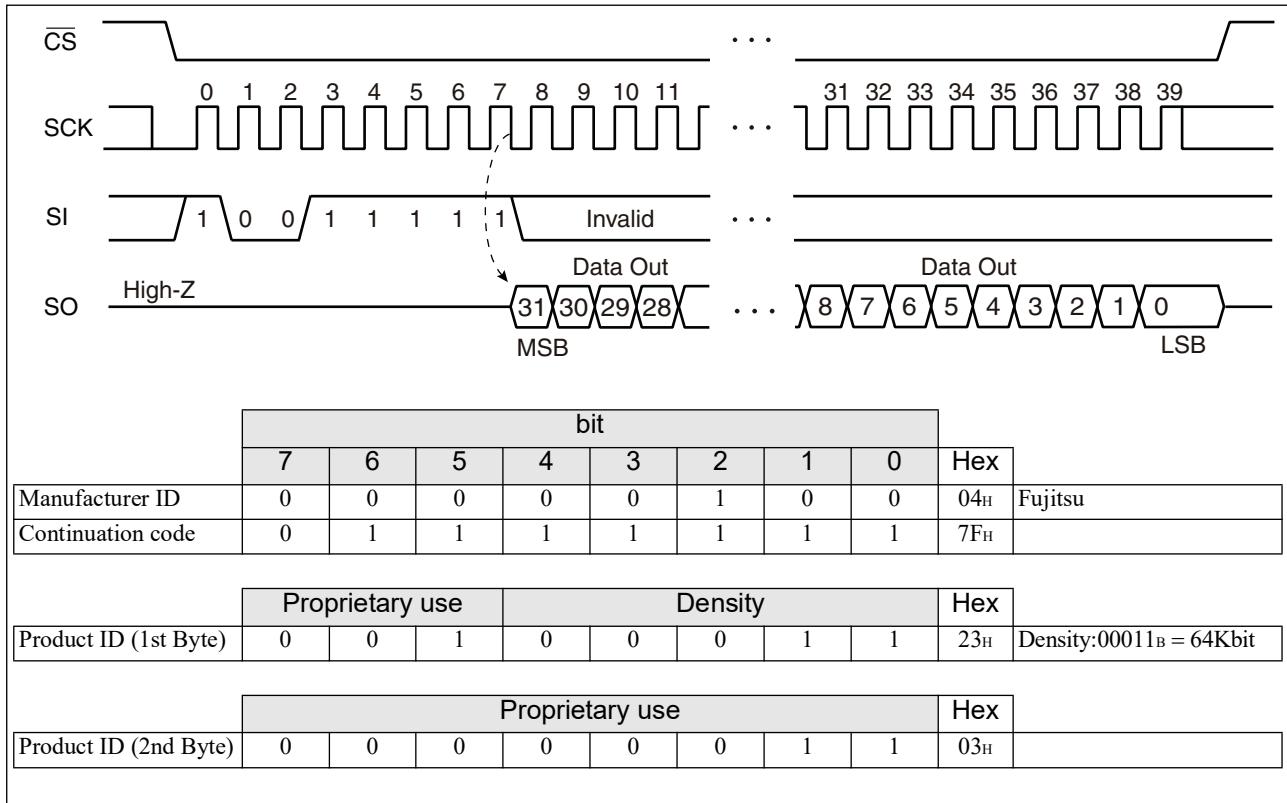
• WRITE

The WRITE command writes data to FeRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The 3-bit upper address bit is invalid. When 8 bits of writing data is input, data is written to FeRAM memory cell array. Risen \overline{CS} will terminate the WRITE command. However, if you continue sending the writing data for 8 bits each before \overline{CS} rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle keeps on continued infinitely.



• RDID

The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until \overline{CS} is risen.

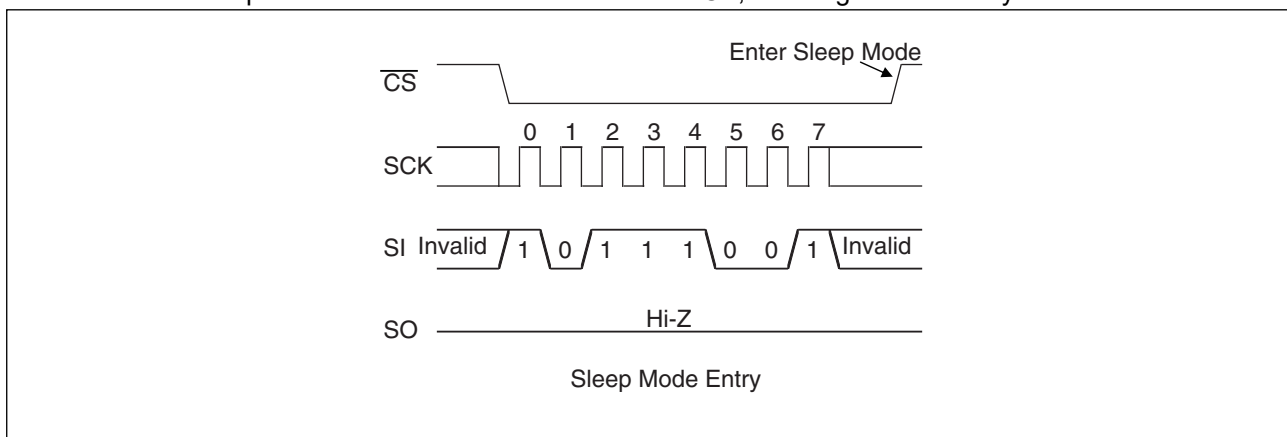


• SLEEP

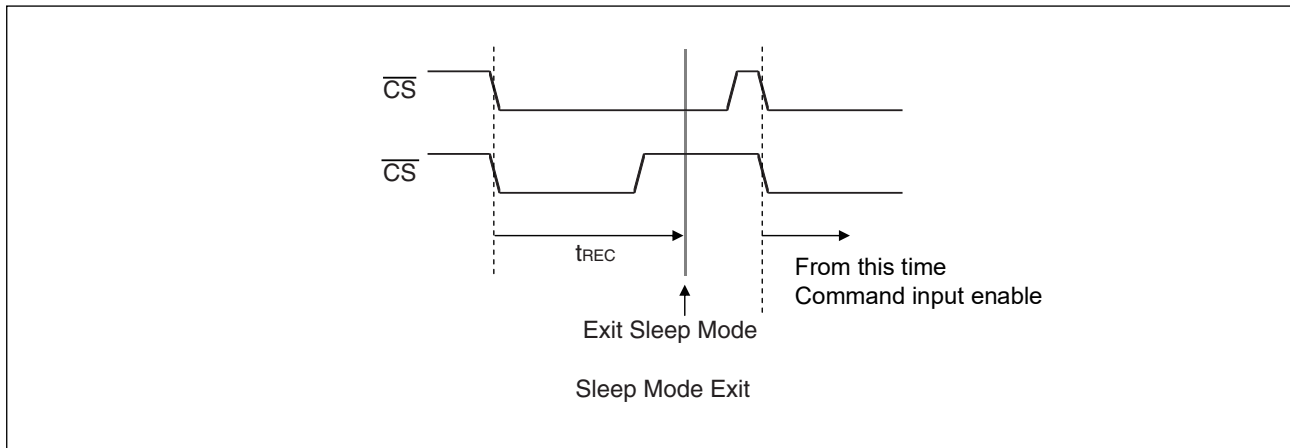
The SLEEP command shifts the LSI to a low power mode called "SLEEP mode". The transition to the SLEEP mode is carried out at the rising edge of \overline{CS} after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of \overline{CS} after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are logically ignored and SO changes to a Hi-Z state.

In case all other pins are not fixed to VDD or VSS than \overline{CS} , a through-current may flow.



Returning to a normal operation from the SLEEP mode is carried out after t_{REC} (Max 400 μ s) time from the falling edge of \overline{CS} (see the figure below). It is possible to return \overline{CS} to H level before t_{REC} time. However, it is prohibited to bring down \overline{CS} to L level again during t_{REC} period.



■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	1800 _H to 1FFF _H (upper 1/4)
1	0	1000 _H to 1FFF _H (upper 1/2)
1	1	0000 _H to 1FFF _H (all)

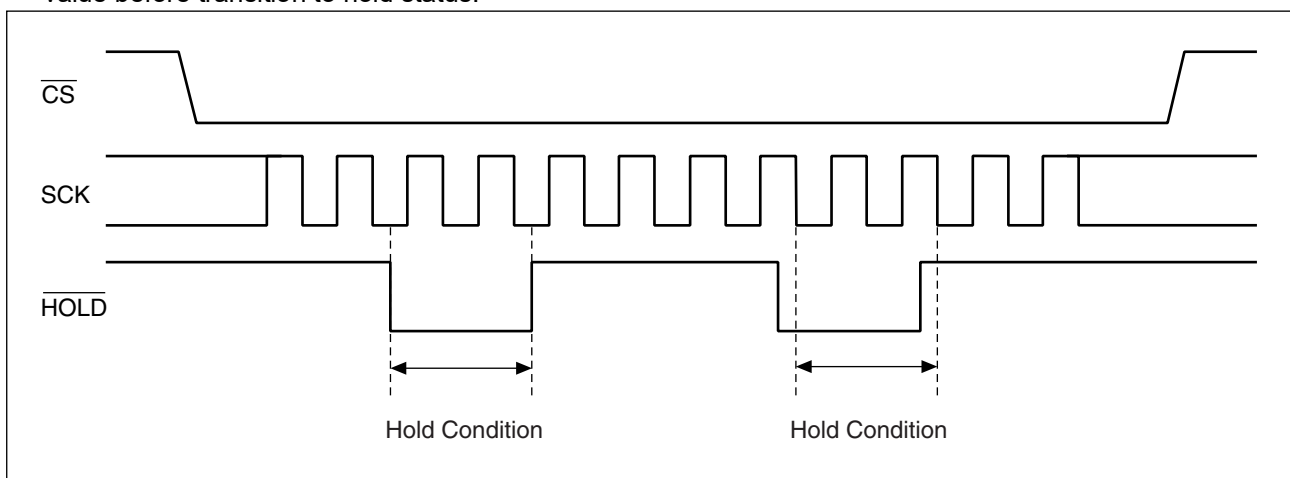
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, WP as shown in the table.

WEL	WPEN	WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{\text{HOLD}}$ is the "L" level while $\overline{\text{CS}}$ is the "L" level. The timing for starting and ending hold status depends on the SCK to be the "H" level or the "L" level when a HOLD pin input is transitioned to the hold condition as shown in the diagram below. In case the $\overline{\text{HOLD}}$ pin transitioned to "L" level when SCK is "L" level, return the $\overline{\text{HOLD}}$ pin to "H" level at SCK being "L" level. In the same manner, in case the $\overline{\text{HOLD}}$ pin transitioned to "L" level when SCK is "H" level, return the $\overline{\text{HOLD}}$ pin to "H" level at SCK being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become don't care. And, SO becomes High-Z while reading command (RDSR, READ). If $\overline{\text{CS}}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	- 0.5	+ 4.0	V
Input voltage*	V_{IN}	- 0.5	$V_{DD} + 0.5$	V
Output voltage*	V_{OUT}	- 0.5	$V_{DD} + 0.5$	V
Operation ambient temperature	T_A	- 40	+ 85	°C
Storage temperature	T_{stg}	- 55	+ 125	°C

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage* ¹	V_{DD}	1.7	3.3	3.6	V
Operation ambient temperature* ²	T_A	- 40	—	+ 85	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

MB85RS64T

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	$ I_{LI} $	\overline{WP} , \overline{HOLD} , \overline{SCK} , \overline{CS} , $SI = 0\text{ V to }V_{DD}$	—	—	1	μA
Output leakage current*2	$ I_{LO} $	$SO = 0\text{ V to }V_{DD}$	—	—	1	μA
Operating power supply current	I_{DD}	$SCK = 0.1\text{MHz}$	—	15	—	μA
		$SCK = 1\text{ MHz}$	—	60	100	μA
		$SCK = 10\text{ MHz}$	—	500	800	μA
Standby current	I_{SB}	$SCK = SI = \overline{CS} = V_{DD}$	—	9	12	μA
Sleep current	I_{ZZ}	$\overline{CS} = V_{DD}$ all inputs V_{SS} or V_{DD}	—	4	6	μA
Input high voltage	V_{IH}	$V_{DD} = 1.7\text{ V to }3.6\text{ V}$	$V_{DD} \times 0.7$	—	$V_{DD} + 0.5$	V
Input low voltage	V_{IL}	$V_{DD} = 1.7\text{ V to }3.6\text{ V}$	-0.5	—	$V_{DD} \times 0.3$	V
Output high voltage	V_{OH}	$I_{OH} = -2\text{ mA}$	$V_{DD} - 0.5$	—	V_{DD}	V
Output low voltage	V_{OL}	$I_{OL} = 2\text{ mA}$	V_{SS}	—	0.4	V

*1: Applicable to; \overline{CS} , \overline{WP} , \overline{HOLD} , \overline{SCK} , SI

*2: Applicable to; SO

*1

2. AC Characteristics

Parameter	Symbol	Value		Unit
		Min	Max	
SCK clock frequency	f _{CK}	0	10	MHz
Clock high time	t _{CH}	20	—	ns
Clock low time	t _{CL}	20	—	ns
Chip select set up time	t _{CSU}	10	—	ns
Chip select hold time	t _{CSH}	10	—	ns
Output disable time	t _{OD}	—	12	ns
Output data valid time	t _{ODV}	—	18	ns
Output hold time	t _{OH}	0	—	ns
Deselect time	t _D	40	—	ns
Data rising time	t _R	—	50	ns
Data falling time	t _F	—	50	ns
Data set up time	t _{SU}	5	—	ns
Data hold time	t _H	5	—	ns
$\overline{\text{HOLD}}$ set up time	t _{HS}	10	—	ns
$\overline{\text{HOLD}}$ hold time	t _{HH}	10	—	ns
$\overline{\text{HOLD}}$ output floating time	t _{HZ}	—	20	ns
$\overline{\text{HOLD}}$ output active time	t _{LZ}	—	20	ns
SLEEP resume time	t _{REC}	—	400	μs

AC Test Condition

Power supply voltage : 1.7 V to 3.6 V

Operation ambient temperature : - 40 °C to + 85 °C

Input voltage magnitude : $0 \leq V_{IL} \leq 0.3 \times V_{DD}$, $0.7 \times V_{DD} \leq V_{IH} \leq V_{DD}$.

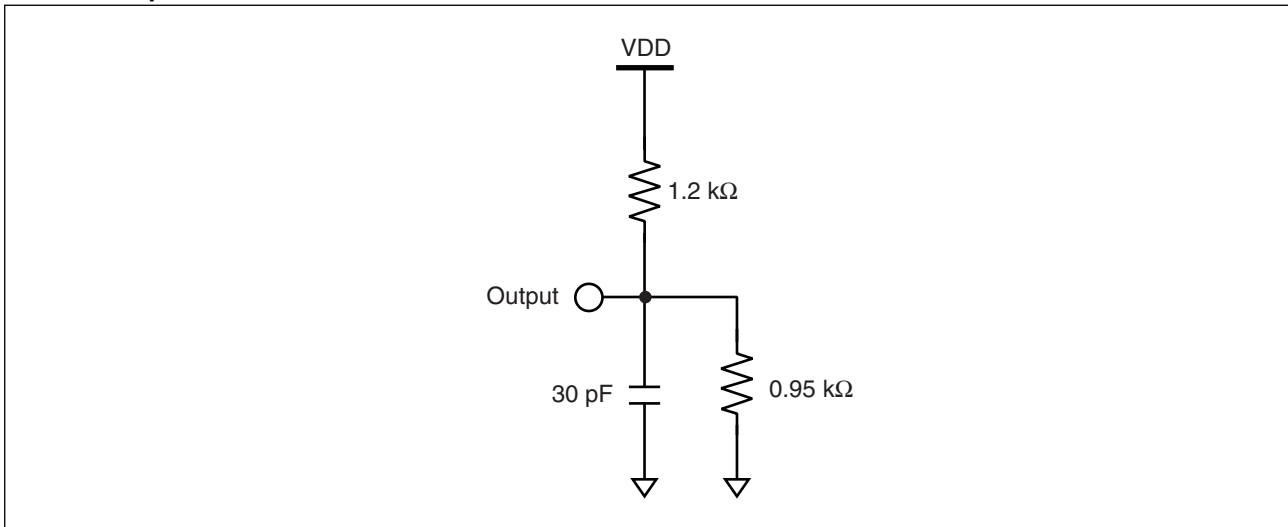
Input rising time : 5 ns

Input falling time : 5 ns

Input judge level : $V_{DD}/2$

Output judge level : $V_{DD}/2$

AC Load Equivalent Circuit

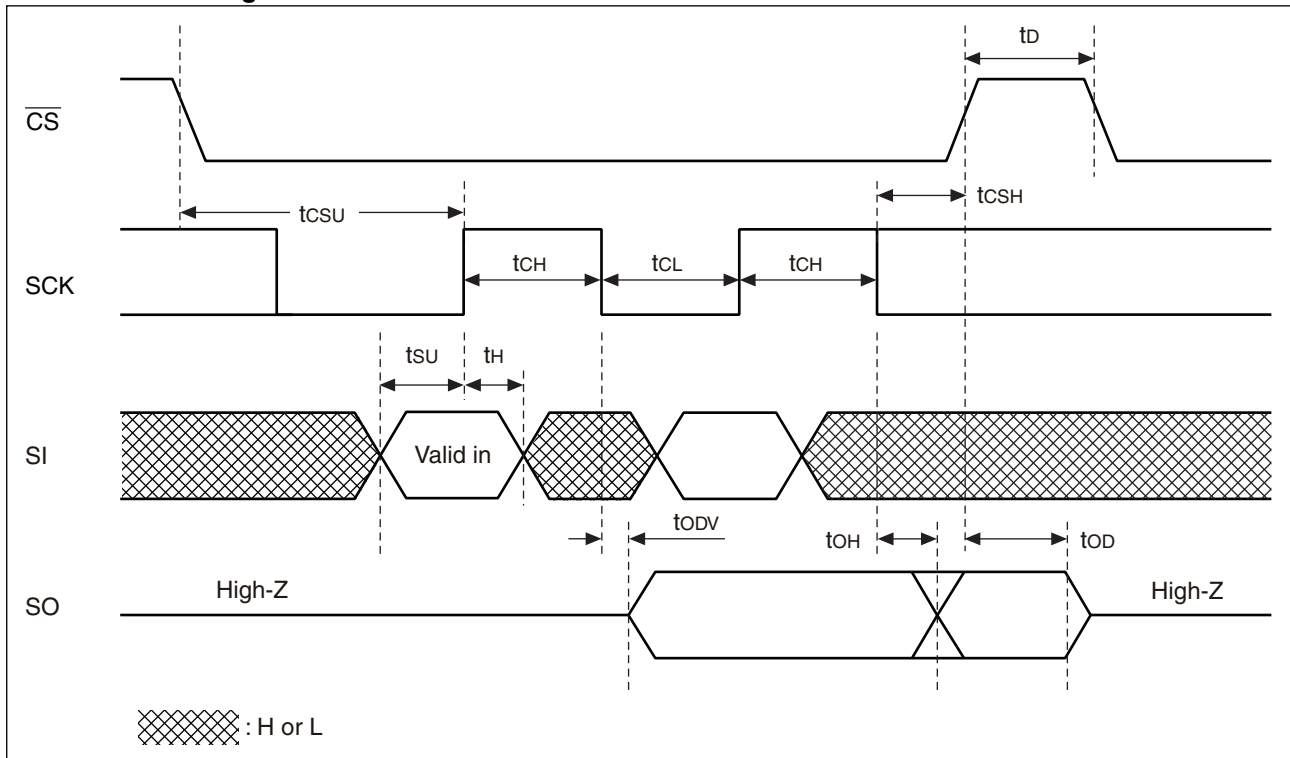


3. Pin Capacitance

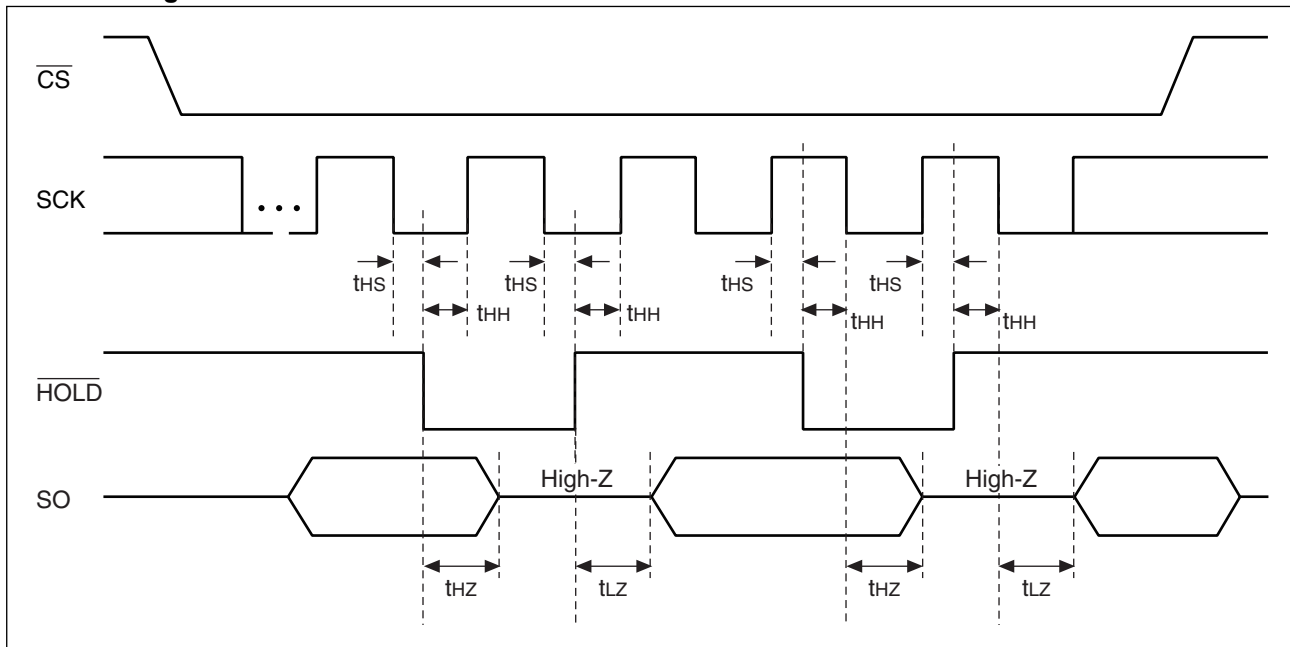
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Output capacitance	C_o	$V_{DD} = V_{IN} = V_{OUT} = 0\text{ V}$ $f = 1\text{ MHz}, T_A = +25\text{ °C}$	—	8	pF
Input capacitance	C_i		—	6	pF

■ TIMING DIAGRAM

• Serial Data Timing

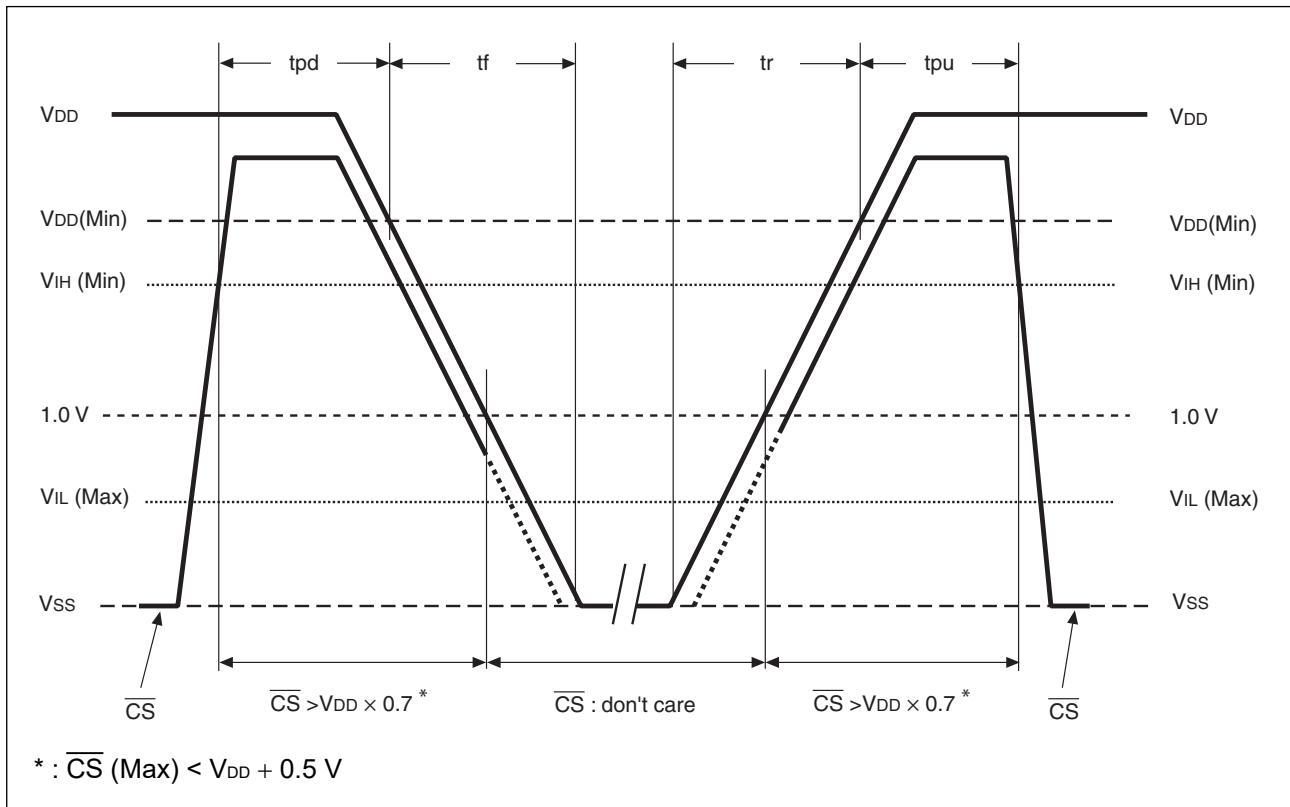


• Hold Timing



MB85RS64T

■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value		Unit
		Min	Max	
\overline{CS} level hold time at power OFF	tpd	400	—	ns
\overline{CS} level hold time at power ON	tpu	250	—	μs
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{13}	—	Times/byte	Operation Ambient Temperature $T_A = +85\text{ }^\circ\text{C}$ Total number of reading and writing.
Data Retention*2	40.2	—	Years	Operation Ambient Temperature $T_A = +85\text{ }^\circ\text{C}$
	383	—		Operation Ambient Temperature $T_A = +55\text{ }^\circ\text{C}$

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

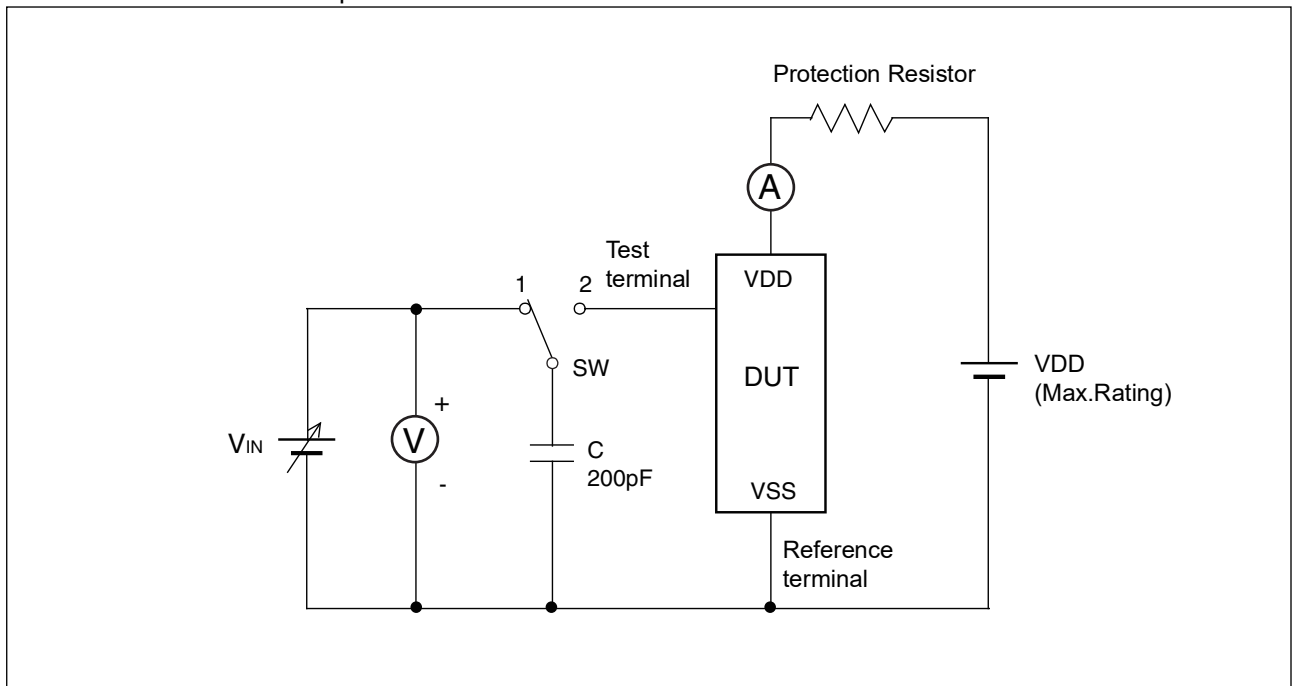
■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RS64TPNF-G-JNE2 MB85RS64TPNF-G-JNERE2	$\geq 2000 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant		$\geq 1000 \text{ V} $
Latch-Up (C-V Method) Proprietary method		$\geq 200 \text{ V} $

- C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

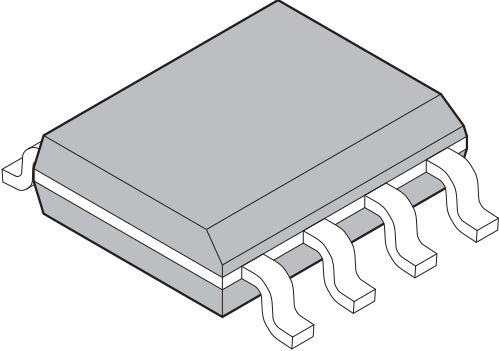
MB85RS64T

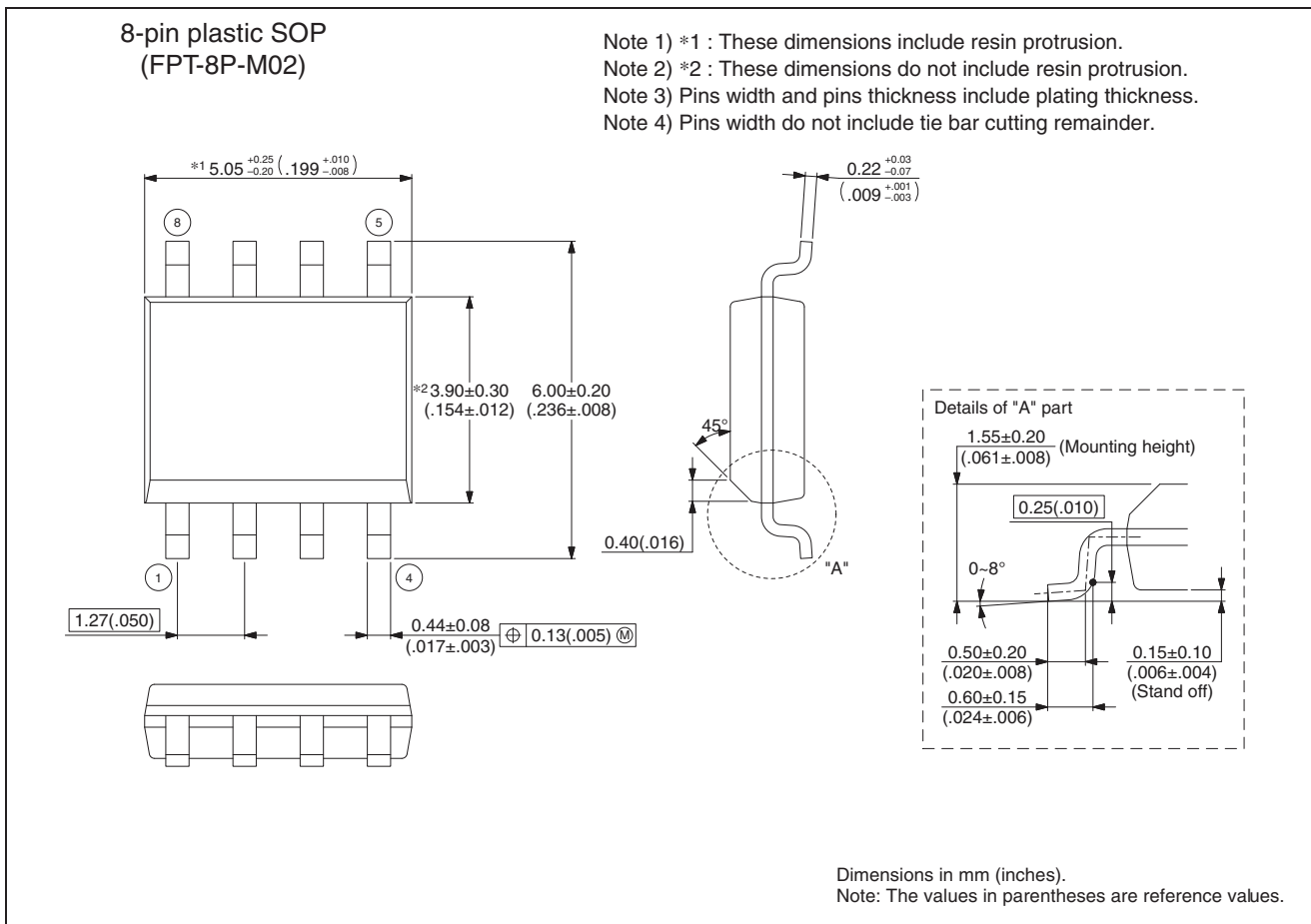
■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RS64TPNF-G-JNE2	8-pin plastic SOP (FPT-8P-M02)	Tube	—*
MB85RS64TPNF-G-JNERE2	8-pin plastic SOP (FPT-8P-M02)	Embossed Carrier tape	1500

*: Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSION

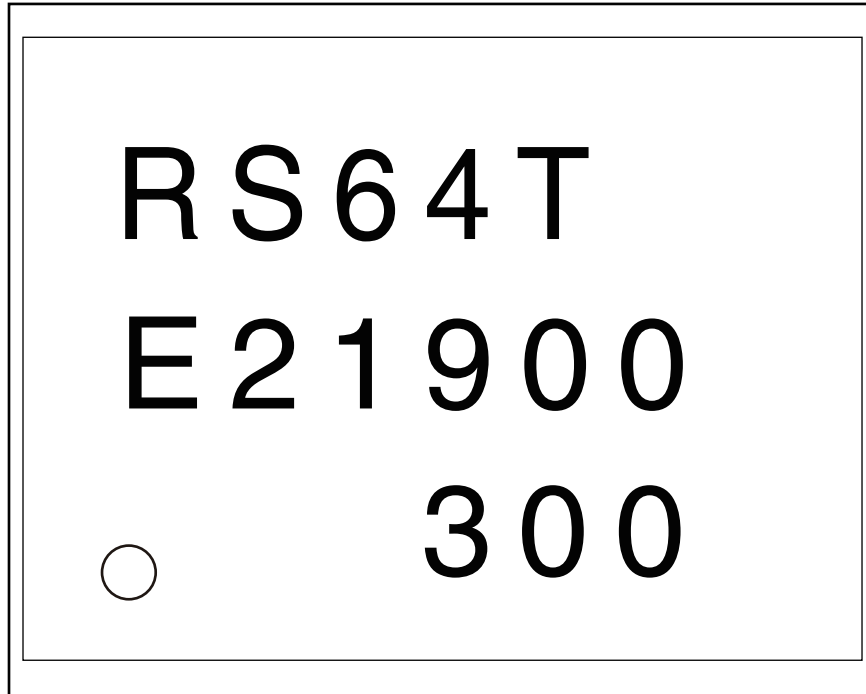
<p>8-pin plastic SOP</p>  <p>(FPT-8P-M02)</p>	Lead pitch	1.27 mm	
	Package width × package length	3.9 mm × 5.05 mm	
	Lead shape	Gullwing	
	Sealing method	Plastic mold	
	Mounting height	1.75 mm MAX	



MB85RS64T

■ MARKING

[MB85RS64TPNF-G-JNE2]
[MB85RS64TPNF-G-JNERE2]



[FPT-8P-M02]

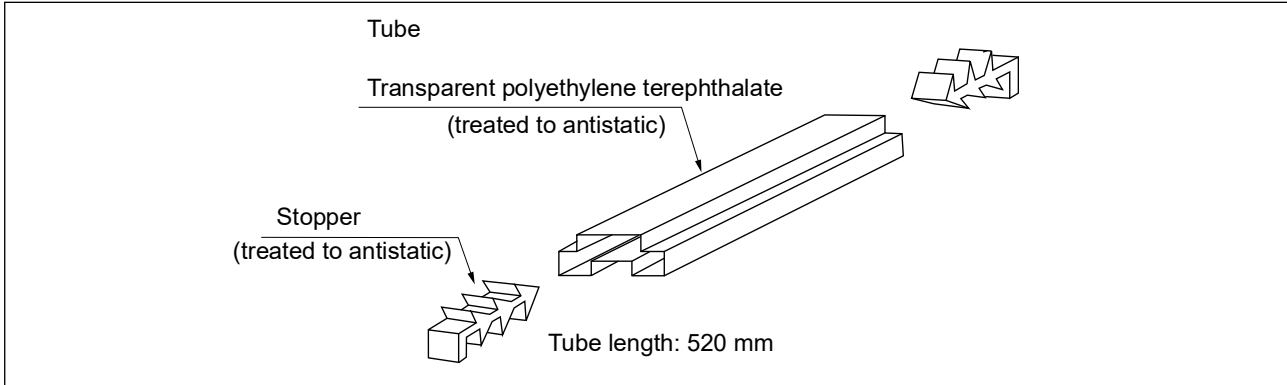
RS64T: Product Name
E2: Lead-free
1900: Year and Week code
300: Reference number

■ PACKING INFORMATION

1. Tube

1.1 Tube Dimensions

- Tube/stopper shape



Tube cross-sections and Maximum quantity

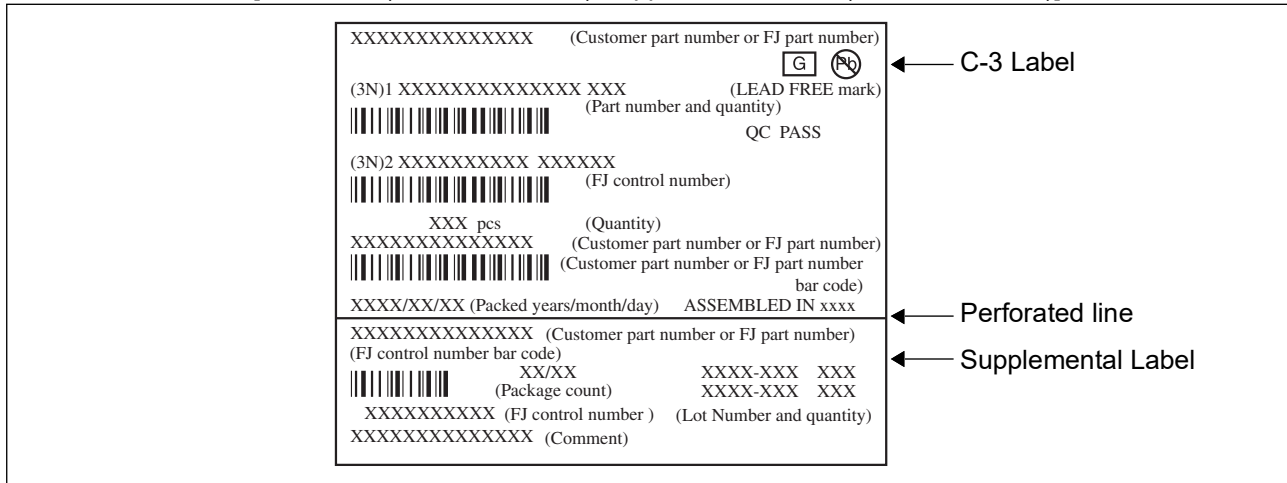
Package form	Package code	Maximum quantity		
		pcs/ tube	pcs/inner box	pcs/outer box
SOP, 8, plastic (2) =	FPT-8P-M02	95	7600	30400
Transparent polyethylene terephthalate				

(Dimensions in mm)

MB85RS64T

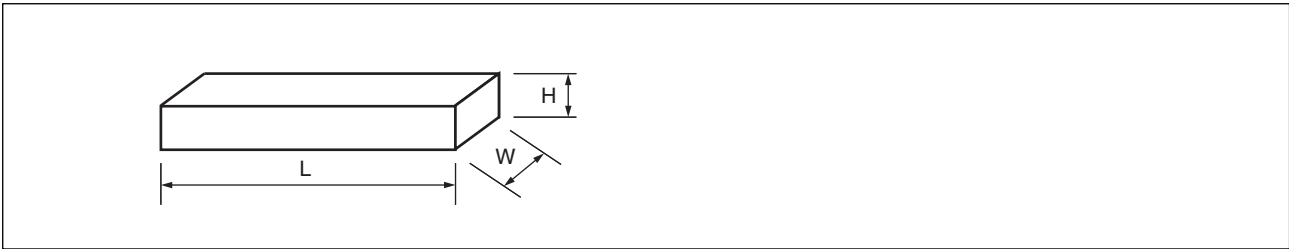
1.2 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



1.3 Dimensions for Containers

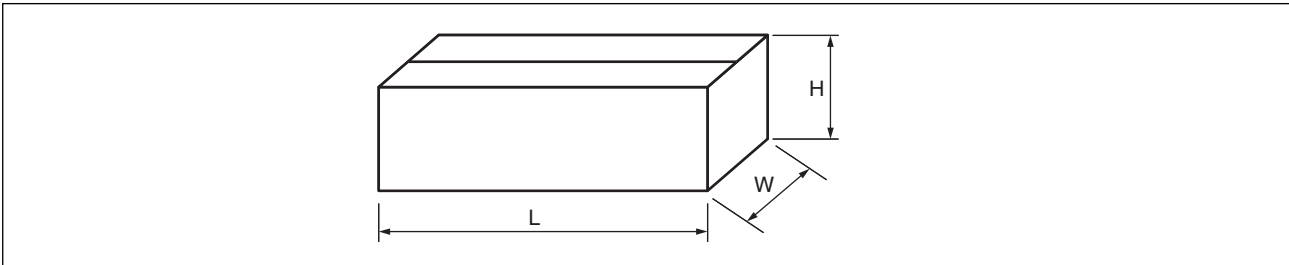
(1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
549	277	180

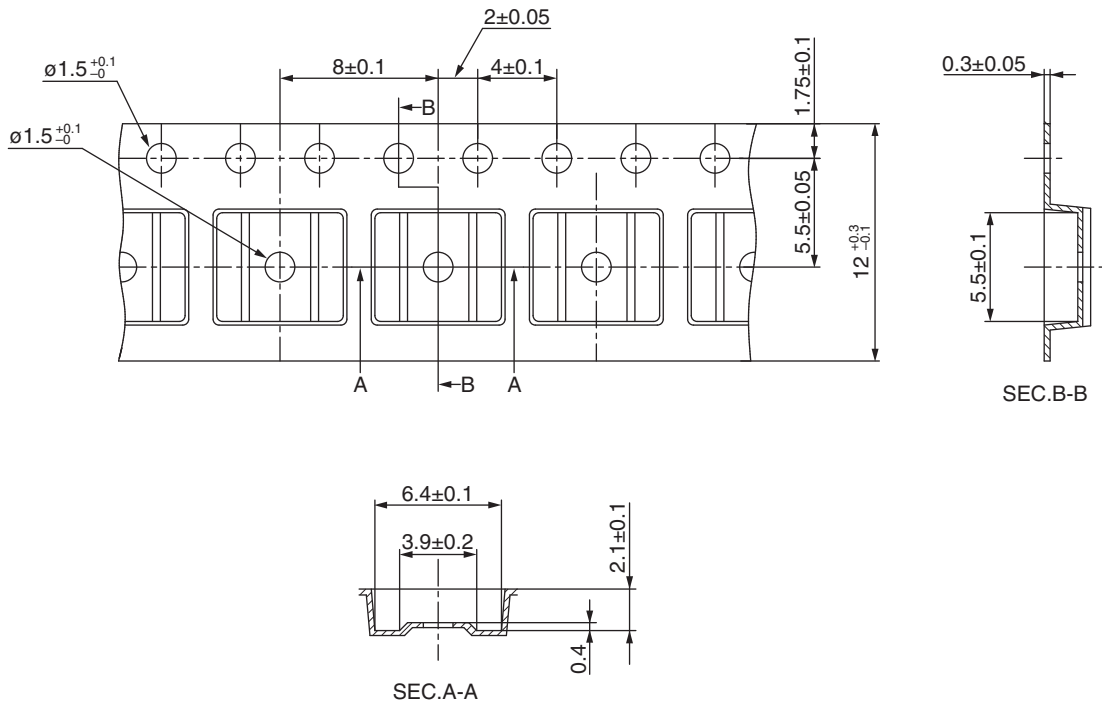
(Dimensions in mm)

MB85RS64T

2. Emboss Tape

2.1 Tape Dimensions

PKG code	Reel No	Maximum storage capacity		
		pcs/reel	pcs/inner box	pcs/outer box
FPT-8P-M02	3	1500	1500	10500



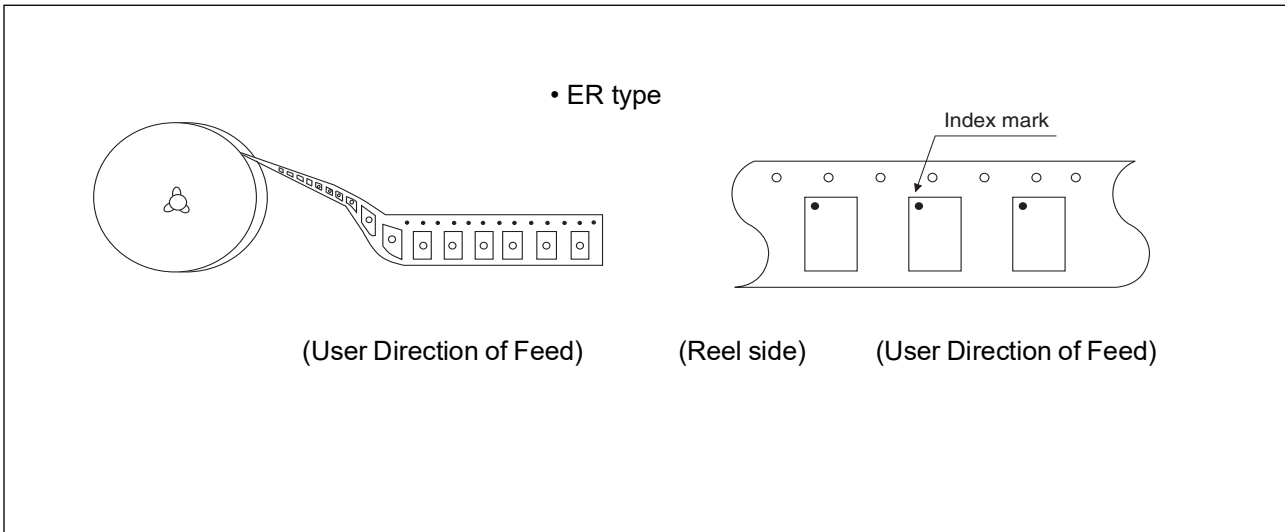
(Dimensions in mm)

Material : Conductive polystyrene

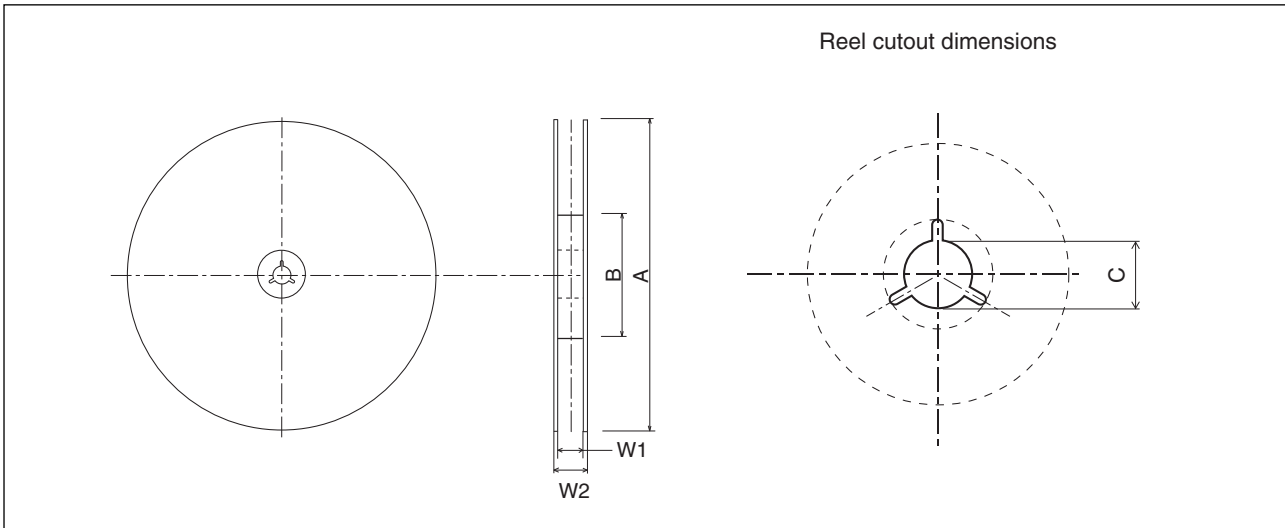
Heat proof temperature : No heat resistance.

Package should not be baked
by using tape and reel.

2.2 IC orientation



2.3 Reel dimensions



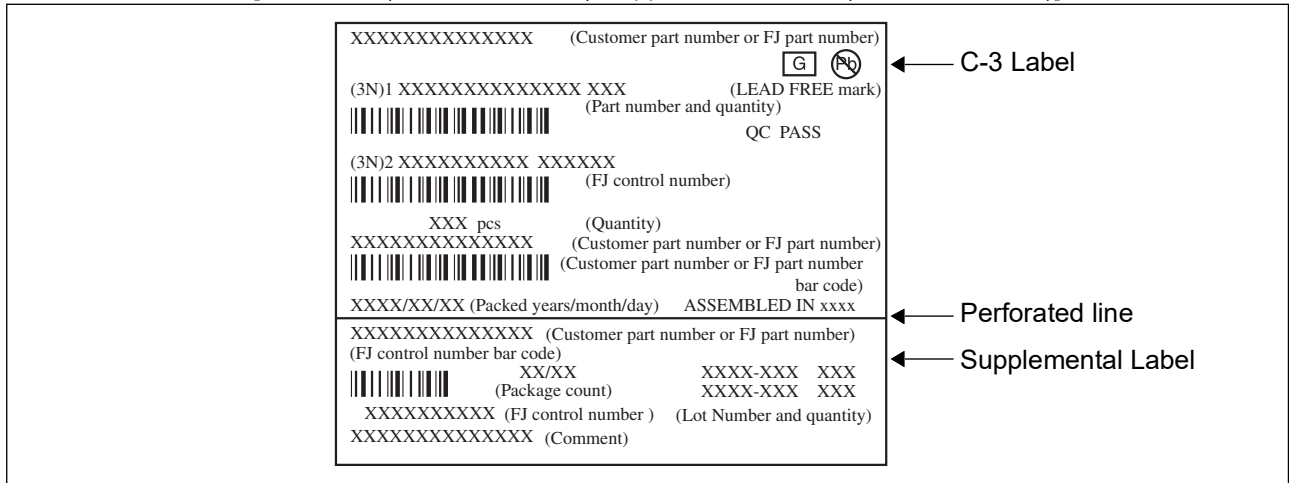
Dimensions in mm

Tape width	A	B	C	W1	W2
12	330	100	13	13.7	17.5

MB85RS64T

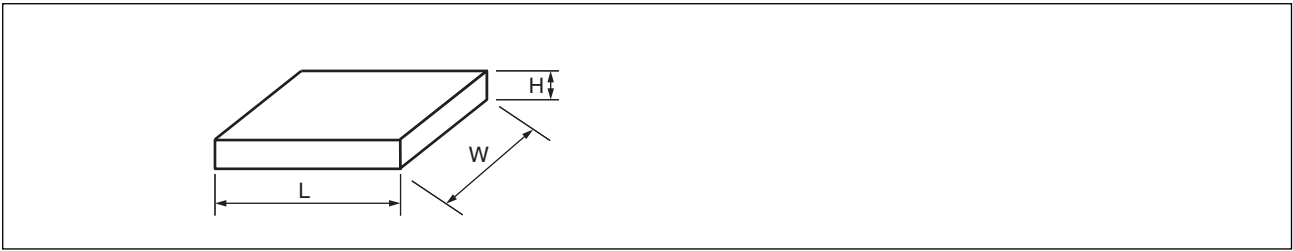
2.4 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
 [C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



2.5 Dimensions for Containers

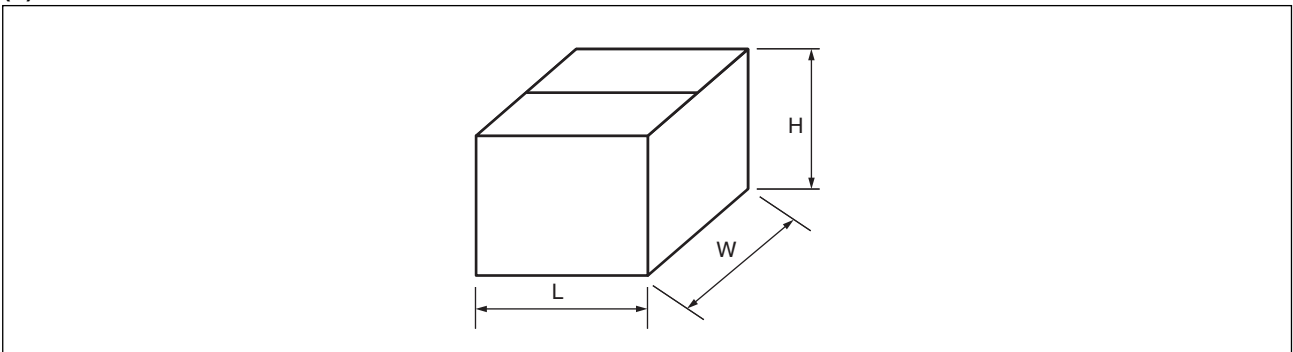
(1) Dimensions for inner box



Tape width	L	W	H
12	365	345	40

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
415	400	315

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

Changes on pages are indicated by vertical lines drawn on the left side of that pages.

Page	Section	Change Results
—	Overall	Following technical word is revised to more commonly used one. FRAM to FeRAM

MB85RS64T

RAMXEED LIMITED

Shin-Yokohama Chuo Building, 2-100-45 Shin-Yokohama,

Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan

<https://ramxeed.com/>

All Rights Reserved.

RAMXEED LIMITED, its subsidiaries and affiliates (collectively, "RAMXEED") reserves the right to make changes to the information contained in this document without notice. Please contact your RAMXEED sales representatives before order of RAMXEED device.

Information contained in this document, such as descriptions of function and application circuit examples is presented solely for reference to examples of operations and uses of RAMXEED device. RAMXEED disclaims any and all warranties of any kind, whether express or implied, related to such information, including, without limitation, quality, accuracy, performance, proper operation of the device or non-infringement. If you develop equipment or product incorporating the RAMXEED device based on such information, you must assume any responsibility or liability arising out of or in connection with such information or any use thereof. RAMXEED assumes no responsibility or liability for any damages whatsoever arising out of or in connection with such information or any use thereof.

Nothing contained in this document shall be construed as granting or conferring any right under any patents, copyrights, or any other intellectual property rights of RAMXEED or any third party by license or otherwise, express or implied. RAMXEED assumes no responsibility or liability for any infringement of any intellectual property rights or other rights of third parties resulting from or in connection with the information contained herein or use thereof.

The products described in this document are designed, developed and manufactured as contemplated for general use including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high levels of safety is secured, could lead directly to death, personal injury, severe physical damage or other loss (including, without limitation, use in nuclear facility, aircraft flight control system, air traffic control system, mass transport control system, medical life support system and military application), or (2) for use requiring extremely high level of reliability (including, without limitation, submersible repeater and artificial satellite). RAMXEED shall not be liable for you and/or any third party for any claims or damages arising out of or in connection with above-mentioned uses of the products.

Any semiconductor devices fail or malfunction with some probability. You are responsible for providing adequate designs and safeguards against injury, damage or loss from such failures or malfunctions, by incorporating safety design measures into your facility, equipments and products such as redundancy, fire protection, and prevention of overcurrent levels and other abnormal operating conditions.

The products and technical information described in this document are subject to the Foreign Exchange and Foreign Trade Control Law of Japan, and may be subject to export or import laws or regulations in U.S. or other countries. You are responsible for ensuring compliance with such laws and regulations relating to export or re-export of the products and technical information described herein.

All company names, brand names and trademarks herein are property of their respective owners.